Daily Briefing: *News Snippets*

Military EMBEDDED SYSTEMS

VOLUME 6 NUMBER 2
MAR/APR 2010

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Tough enough? Mil PSU says *Ooh-Rah!*

Also:

Ex-CIA expert extols cloud computing

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Supplement inside:
MIL/COTS DIGEST
Rugged SFFs

Military EMBEDDED SYSTEMS

March/April 2010 Volume 6 Number 2

COLUMNS

DEPARTMENTS

ON THE COVER:

A slightly less recognized image of the famous Iwo Jima flag raising where a small flag carried ashore by the 2d Battalion, 28th Marines is planted atop Mount Suribachi at 1020, 23 February 1945. As the Americans island hopped across the Pacific towards the end of WWII, Iwo Jima was one of the last enemy islands to fall – though at horrific loss of life to the Allies and to the enemy. Men on both sides were as tough as they come, and the editors of *Military Embedded Systems* are in awe of their sacrifices. To the left of the image is the brand-new 2010 U.S. Postal Service stamp honoring the event.

"Tough" is the theme of this special *Embedded Systems Conference* issue of *MES*. The articles on rugged uninterruptible power supplies (page 48) and on chassis heat dissipation (page 24) characterize tough COTS electronic designs.

(Photo courtesy of Wikipedia and Staff Sergeant Louis R. Lowery, USMC, staff photographer for "Leatherneck" magazine. Postage stamp image courtesy of Wikipedia and the United States Postal Service.)

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Enhancing target tracking in critical applications

By Duncan Young

Electro-Optical (EO) sensors continue to evolve in performance and resolution, requiring more signal processing power for better target discrimination, lower error rates, and improved accuracy. Automatic target tracking enables the sensor subsystem to identify and track multiple targets through clutter, weather, atmospheric disturbances, and countermeasures designed to obscure the target or seduce the sensor. At the platform level such as a combat aircraft, armored vehicle, or helicopter, it is often proposed that target tracking could be performed as a software task by an integrated central computing resource, receiving raw sensor data from an array of sensor types. Compared to a dedicated, embeddable hardware solution, this architecture requires considerable general-purpose processing power. However, by using the latest generation of low-power, mixed media processing devices developed for the 3G smartphone market, an embedded tracker can be optimized for both performance and a platform's vital Size, Weight, and Power (SWaP) characteristics.

Target tracking

EO sensors are used extensively in ground-to-air, air-to-air, and air-to-ground fire control systems, surveillance, security, and perimeter defense systems. Sensor images are processed by a tracking system to identify and follow objects such as aircraft, vehicles, or personnel that are moving within a set of prescribed characteristics for those particular types of objects. Automatic tracking is often a requirement as it provides low error rates and consistent performance and does not suffer the same fatigue or stress as a man-in-the-loop. A typical tracker has three functional stages:

- Preprocessing the incoming video stream at the pixel level for contrast and statistically based enhancement
- Image analysis to identify objects of interest within defined areas or windows
- Analysis of objects' movement over a number of frames to identify them as tracks, which are then followed using predictive algorithms to confirm their progress.

The complexity of the tracking function varies considerably from a fixed-position tracker for a single target fire control system, to a tracker on a highly maneuverable airborne platform such as an Unmanned Aerial Vehicle (UAV) or helicopter, required to track multiple ground-based moving targets. Many tracking applications, such as ground attack aircraft or helicopters, are closed-loop systems whereby the sensor and/or a weapons system must follow a designated target track. This requires rapid loop response time and hence dedicated high-performance processing to maintain lock on the target if the sensor platform and target are both moving.

3G mobile telephony provides key technology source

Sensor technology continues to evolve rapidly, requiring a comparable increase in signal processing power as pixel count, frame rates, and analog-to-digital conversion resolutions increase. Recent higher-resolution sensors transmit video in digital formats, including CameraLink, DVI, HD-SDI, or GbE Vision. The raw digital video data might contain a large amount of noise or clutter or have poor contrast. This often applies across the whole image, so a highly parallel processing device such as an FPGA is well suited to filtering the content, leaving more clearly distinguishable target data for detailed analysis.

Sophisticated tracking and classification algorithms applied to the reduced data set require the greater processing capability of a DSP device. GE Intelligent Platforms' ADEPT 5000 high-performance, embeddable tracker combines these key FPGA, DSP, and 3G smartphone computing technologies to create a rugged, core tracking module small enough to be mounted on a PC/104-*Plus* sized (3.6 x 3.8 inches, 90 x 96 mm) I/O base card (Figure 1). These tracking modules can be attached to many open-standards I/O base card formats such as VPX, VMEbus, PC/104-*Plus*, PCI, or PCI Express. They enable construction of a complete embeddable tracking subsystem that could be colocated with the sensor or embedded as part of the platform's mission computing or display processing resources.

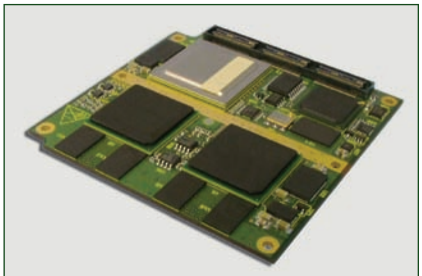
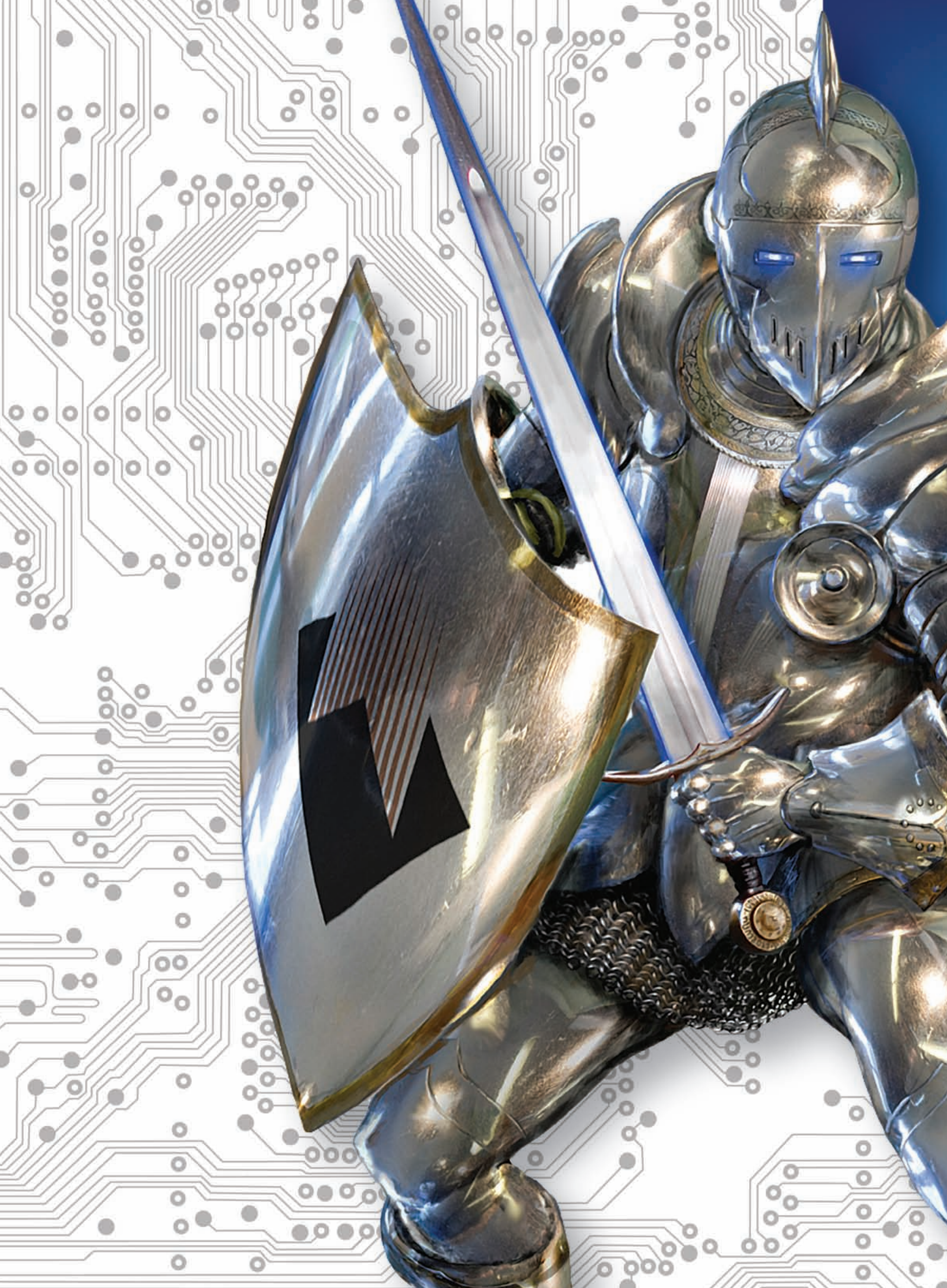


Figure 1 | The ADEPT 5000 high-performance tracker from GE Intelligent Platforms

Enhanced sensor platforms meet today's demands

Ongoing budget concerns continue to restrict new platform development, favoring instead the enhancement and life extension of existing platforms. New or upgraded EO sensors are planned to provide these platforms with vital new operational performance. Advances in tracker capability are helping to hone this edge with the successful infusion of cross-market technology; this results in a complete dedicated tracking subsystem occupying a significantly smaller footprint than a comparable general-purpose embedded computing module, while consuming less than one-third of the power.

To learn more, e-mail Duncan at duncan_young1@sky.com.



Rugged mission displays for surveillance applications

By Steve Edwards

Helicopters and light aircraft are used extensively for policing, homeland security, border control, drug interdiction, and many other forms of aerial surveillance by both military and civilian organizations. Equipped with a range of Electro-Optical (EO) sensors such as low-light TV, Forward Looking Infrared (FLIR), and a new generation of High Definition TV (HDTV) cameras, these aircraft have mission-system capability to display, process, and record sensor data independent of their flight-safety critical avionics systems. Mission data and real-time sensor images are displayed to operators and flight crew on rugged flat panel displays. By incorporating direct operator input via touch screen and soft keys, plus video switching and windowing within each display unit itself, a mission system can be configured cost effectively and flexibly using off-the-shelf rugged computing components.

Video switching and display

Mission display systems have evolved rapidly from a model of one sensor feeding one display to multisensor, multiple display systems needing complex video distribution, switching, and cabling with additional requirements for recording and uplink/downlink communications. Typically a multisensor system will have two or three operator positions, each with more than one screen. Each operator can select from any – or a number of – video sources from the sensor suite, other operators, or computer generated graphics such as maps or uplinked images. The chosen method of video distribution might also need to connect the sensor video to the mission computing system for tracking or other image processing tasks prior to display. Recording must also be selectable from any of the screens or the sensors or computing system.

This need for flexibility calls for considerable quantities of cables and a video switching subsystem to provide for all the possible routing and video formats, such as analog or digital (DVI). Architecturally, multisensor mission systems have made use of a separate, very complex video switching and distribution subsystem to interconnect various permutations of sensors, mission computers, and display screens. However, by combining many of the switching and display functions such as picture-in-picture and multiple sensor windows with the ability to route sensor images to other operator positions within the display itself, appreciable savings in cost, cable space, weight, and complexity can be achieved.

Typically an operator will interact with the mission system using a range of input devices such as a keyboard, function keys, pointing devices, and a touch screen. The Man Machine Interface (MMI) is most often handled by the mission computer as a set of discrete functional devices; every key press or command input requires processing and consequent action to be taken. Many such operator MMI functions include switching video sources, creating multiple windows, or pointing or dragging images using the touch screen and requiring no assistance from the mission computing system for their operation.

Mission displays integrate switching and MMI

This class of multisensor surveillance systems relies heavily on direct operator interpretation of incoming images, sensor selection, and viewing characteristics while the mission computing system performs mission management functions independently of the image content or operator's surveillance task. However, the mission computer might be providing logistical or tactical data such as the disposition of resources on the ground, or digital maps that can be selected and displayed by the operators. This is typical of a helicopter-borne police surveillance application. This platform also offers ample space for both operators and flight crew, enabling the use of larger screens in 16:9 format for the display of high definition images or for multiple windows of lower resolution on a single screen. A new breed of rugged mission display is emerging that is ideally suited to these types of applications. These new displays provide integrated, extendable video windowing and switching capability controlled by programmable soft keys and touch-screen input, which – when paired with a rugged laptop-type PC – offers extensive mission system functionality. An example of such a helicopter-based police surveillance system using widescreen 20-inch mission displays supplied by Curtiss-Wright Controls, Embedded Computing (CWCEC) is depicted in Figure 1.

Figure 1 | A helicopter-based police surveillance system uses widescreen 20-inch mission displays.

By integrating a sensor display device with video switching and distribution plus programmable display control functions, the resultant mission display becomes a highly functional but economical mission system building block. Already proven in helicopter and light aircraft surveillance roles, this architecturally flexible approach is well suited to many similar applications such as coastal or fishery protection, operator positions for remotely operated ground and underwater vehicles, and Unmanned Aerial Vehicle (UAV) ground stations.

To learn more, e-mail Steve at Steve.Edwards@curtisswright.com.

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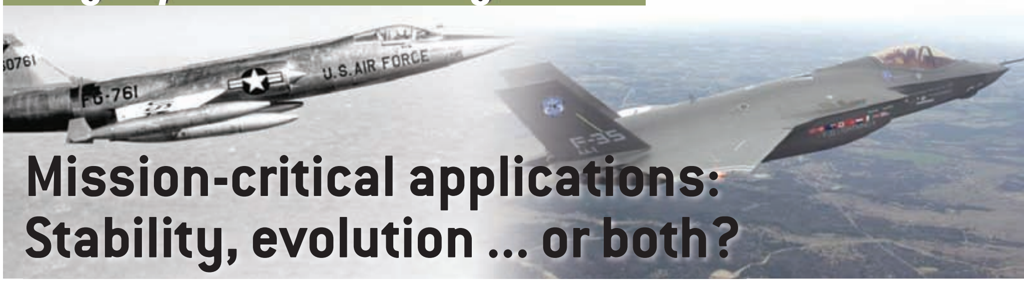
By Tyson Moler



Mission-critical applications: Stability, evolution ... or both?

Due to long budget cycles and a growing deficit, defense systems must adapt to evolving threats by refreshing their current infrastructure while bolting on new capabilities to meet rising High Availability (HA) requirements. Open standards routes such as the Service Availability Forum's (SA Forum's) Availability Management Framework (AMF), along with COTS software, offer the best opportunities to successfully meet this challenging paradox.

There is a tremendous investment in existing mission-critical applications. As they become networked, their criticality to the overall mission increases. Missions also change, raising the system status to mission critical. The net result is that aging systems are being tapped to perform at much greater levels of operational availability than their original designs intended.

The defense community has come to see open standards-based COTS technology as a solution to this life-cycle challenge. Historically, no open standard has addressed system-wide fault management and operational availability. Existing high availability infrastructures are often proprietary and difficult to adapt. COTS software helps deal with both of these issues, and also satisfies the need for unified and flexible management of system configurations.

The benefits of the open standards COTS approach to operational availability go beyond meeting current mission requirements. Future evolution is enabling – and enabled – in two important ways. First, it enables the applications to be transportable across platforms and eases the integration of future capabilities. Second, unified configuration management provides a faster and simpler approach to implementing new components and capabilities. Accordingly, the Service Availability Forum's (SA Forum's) Availability Management Framework (AMF) is working to support today's mission-critical High Availability (HA) needs while also outlining numerous approaches to ease legacy software migration.

AMF and mission-critical HA

The SA Forum is a commercial software consortium that has produced a set of open standards that addresses mission-critical requirements for software-based systems with nearly real-time/real-time applications. The SA Forum has always been sensitive to the issue of legacy application support, and members of the group have identified a spectrum of support paradigms. They have additionally formalized various software redundancy schemes that support HA. The SA Forum's work is now being implemented by the U.S. Navy and is a DoD-wide mandated specification in the DoD IT Standards Registry (DISR).

The SA Forum specifically provides an AMF service that supports subsecond software redundancy and fault management capabilities that satisfy the mission-critical requirement. AMF involves a system model that explains active/standby/spare component redundancy relationships and the policies that deterministically direct the system through fault detection, isolation, and recovery to ensure continuous service availability. System model particulars are crafted by an insightful system designer at development time. These redundant components manifest in the system as software processes or applications that could be newly developed, third-party, or legacy applications.

New applications are best served by linking in SA Forum service libraries, which provide the most time-sensitive fault detection and failover performance, as this allows for explicit application health monitoring and direct redundancy state assignment (active/standby/spare). However, many third-party or legacy applications cannot change; a nonintrusive integration approach is required.

AMF eases legacy software migration

AMF describes several approaches for legacy software migration, two of which are the Wrapper and Proxy-Proxied methods. External Passive Monitoring also provides a highly capable and nonintrusive method for providing availability services to legacy or third-party applications.

The U.S. Navy Common Processing System (CPS) program, in the context of Advanced Capability Builds (ACBs), is a great example of bringing new infrastructure and applications into an existing combat system environment. The CPS platform is a common computing environment for mission-critical applications, and it utilizes SA Forum-compliant middleware to provide software redundancy and dynamic fault management capabilities. CPS will be deployed in Aegis Modernization/ACB12 in the immediate future, and is expected to support additional combat system programs. This approach will greatly extend the life of Aegis-equipped cruisers and destroyers. The intent of the U.S. Navy Consolidated Afloat Networks and Enterprise Services (CANES) Common Computing Environment (CCE) is to achieve similar benefits.

Meeting the HA/legacy integration challenge

Overall, while legacy software migration is a challenging exercise, it is very possible to evolve mission-critical systems in a stable and evolutionary way. COTS solutions for high availability such as those provided by GoAhead Software and other vendors offer the best approach to these migrations. Open standards such as SA Forum's AMF are paving the way for tomorrow's mission-critical systems by providing for today's HA needs while retaining the ability to ease legacy software migration.

Tyson Moler *is director of federal operations at GoAhead Software. Prior to GoAhead, he worked in management consulting, supporting clients in business development, and program management in federal and defense markets. He holds a B.A. in International Relations from Claremont McKenna College. He can be contacted at tmoler@goahead.com.*

By Sharon Schnakenburg-Hess, Assistant Managing Editor

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January 2010 chip sales up

A rise is a rise, no matter how small or large … as indicated in the Semiconductor Industry Association's (SIA's) recent report. Comparing chip sales in January 2010 ($22.5 billion) to December 2009 ($22.4 billion), the increase is a relatively miniscule .3 percent (Figure 1). However, a comparison of January 2010 to January 2009 ($15.3 billion) shows that chip sales soared a whopping 47.2 percent (see figure again). Strong chip sale niches presently include cell phones, industrial applications, cars, and personal computers. Additionally, George Scalise, SIA president, says 2010 appears brighter than originally projected … maybe. "If the current trends continue, there is upside potential for 2010 growth above our November forecast of $242.1 billion, but a growing global economy driven by consumer purchasing will be key to sustaining these trends."

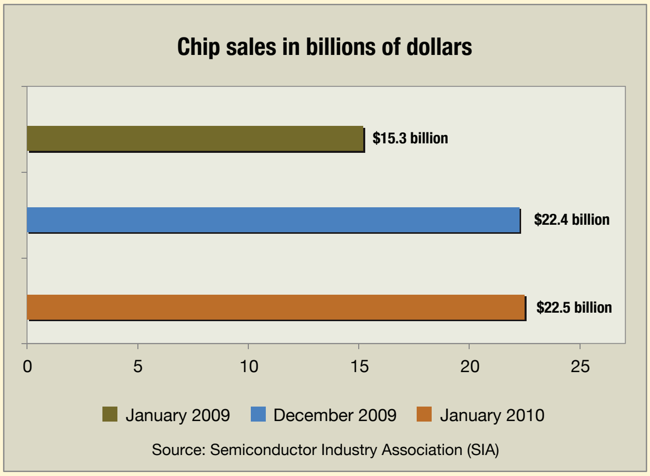

Figure 1 | A comparison of January 2010 to both December 2009 and January 2009 reveals a much larger increase year-to-year than month-to-month.

Northrop Grumman to get the less-glam job done

Though not as glamorous perhaps as designing a system, maintenance and repair are, nevertheless, a necessity … as evidenced by a recent contract between the U.S. Navy's Naval Surface Warfare Center and Northrop Grumman Systems Corp. The $49 million Indefinite Delivery/Indefinite Quantity (IDIQ) contract stipulates that Northrop Grumman provides depot-level maintenance and repairs for several airborne mine countermeasures systems: AN/AQS-24 mine hunting system, CP-2614/T common post-mission analysis, AN/AQS-14A sonar detection set, AN/ALQ-141 acoustic minesweeping/minehunting system, and USM-668 intermediate level test equipment. The contract is slated for fulfillment by February 2015.

KC-130J gets Rolls Royce treatment

On the ground or in the air … Rolls Royce Corp. is almost everywhere, it seems. Between now and February 2011, the company will be lending its technical engineering and contractor logistics services to the KC-130J aircraft – thanks to a $45 million Indefinite Delivery/Indefinite Quantity (IDIQ) contract with the Naval Air Systems Command. Benefitting the Marine Corps, the contract stipulates that Rolls Royce Corp. provides the aforestated services to the KC-130J's propulsion system, comprising the R 391 propeller and the AE 2100D3 turboprop engine.

NASA's Orion gets a forward glance

The recent delivery of the Data Acquisition System (DAS) by G Systems signified *fait accompli* for one of the company's three NASA Orion contracts – and enables NASA future sight capabilities. How? The DAS will compile stress data input from Orion's heat shield structures, Launch Abort System Fairing Assembly (LASFA), Service Module (SM), and crew module (Figure 2) pertaining to strain, torque, and pressure. The data will then enable measurement and simulation of potential space flight, take-off, and re-entry effects. Input from at least 1,400 analog data channels will be collected, analyzed, transferred, stored, and/or viewed at the Orion Structural Test Facility (OSTF). Meanwhile, G Systems' two additional NASA Orion contracts, also facilitated by prime contractor Lockheed Martin, include: 1) the Data Distribution System (DDS), which comprises software and hardware to analyze, distribute, and collect parametric data and video gathered by DAS; and 2) a DAS-integrated computerized vent and pressure system with which the crew module will be tested. The value of the three contracts – which together result in the installation, integration, and design of an automated data analysis/acquisition testing station for Orion – exceeds $1 million. The two remaining contracts are slated for completion by June 2010.

Figure 2 | Orion's crew module, NASA photo by Tony Landis.

Missile Defense Agency proof of concept: 1, 2, 3 ...

While energy is often thought of as dormant and benign, officials at the U.S. Missile Defense Agency would undoubtedly have a different perspective. The reason: A successful proof-of-concept exercise recently demonstrated that directed energy is a viable method of defense against ballistic missiles (Figure 3). The experiment was held at Point Mugu Naval Air Warfare Center-Weapons Division Sea Range near the California coast, where the Airborne Laser Testbed (ALTB) destroyed a "short-range threat-representative ballistic missile" in three steps: First, ALTB's onboard sensors detected the missile and tracked it using a low-energy laser. Second, ALTB fired another low-energy laser in an effort to compensate for and measure atmospheric interference. Third, ALTB shot a high-energy (megawatt-class) laser, heating the missile and resulting in its structural failure. Though ALTB had previously lethally intercepted a solid-fuel missile, this experiment was the first time ALTB destroyed a liquid-fuel missile.

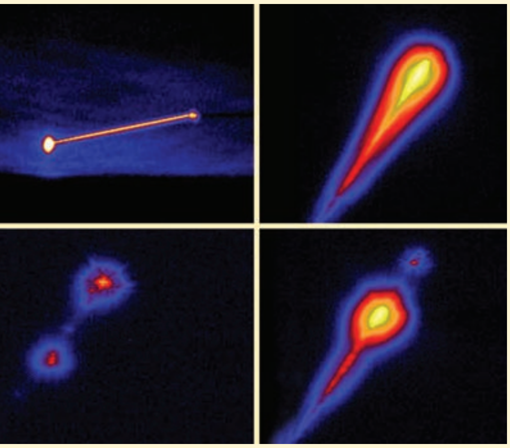

Figure 3 | Upper left photo: An infrared image of the Missile Defense Agency's ALTB (right) destroying a threat-representative short-range ballistic missile (left). Then, clockwise, beginning with photo in upper right corner: The sequence of events in the recent ALTB demonstration. U.S. Missile Defense Agency photos.

Brute force attacks accelerate (obsolete) decryption

Ironically, an obsolete standard has now reached its highest performance levels: Pico Computing claims that its recently reached 56-bit Data Encryption Standard (DES) decryption benchmark speeds represent the highest such levels ever achieved. The enabler: Pico Computing's DES cracking algorithm utilizing FPGAs and 11 Pico EX-Series cards in a 4U server consuming fewer than 1,000 peak watts. Utilizing "brute force methods," the algorithm "iteratively decrypts fixed-size blocks of data to find keys that decrypt into ASCII numbers" to recover encrypted files' keys where the data type is known. In contrast to methods using clustered CPUs (which process 16 million DES key operations per second) or even a PC combined with a 250-million-operations-per-second GPU card, Pico Computing's acceleration yields 1.6 billion DES operations per second for each FPGA. Additionally, a single-server cluster of 176 FPGAs can achieve 280 billion DES operations per second. Thus, the FPGA-enabled DES decryption and resultant key recover can be completed in fewer than three days, while performing the same task on a PC, with or without a GPU, would take years. Though largely replaced with Advanced Encryption Standard (AES) encryption, DES is still used for auditing and developing block-based encryption algorithms and functions in cryptographic research.

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Figure 4 | The USAF and Raytheon recently signed an $886 million contract for improved GPS satellite accuracy via development of the OCX advanced control element. Photo courtesy of Raytheon Company.

USAF/Raytheon: Accuracy is key

The United States Air Force and Raytheon Company recently penned an $886 million contract stipulating that Raytheon incarnates the first two development blocks of a new accuracy-improving element for GPS satellites (Figure 4): The OCX or advanced control segment. The modern service-oriented architecture-based OCX will provide anti-jam capabilities and higher levels of reliability and accuracy than previous GPS. The OCX additionally lends itself to industry and government integration because of its open-system standards base. Providing the public and military with satellite-based radio navigation, the GPS system also comprises the space and user segments. Meanwhile, OCX team members include the Jet Propulsion Laboratory, The Boeing Company, Braxton Technologies, ITT, and Infinity Systems Engineering. The contracting entity is the Air Force Space and Missile Systems Center located at the Los Angeles Air Force Base.

General Dynamics helps DDG 115 "materialize"

The long-awaited DDG 115 destroyer begins to materialize, literally, courtesy of a "not-to-exceed $114,003,000 letter contract" between the U.S. Navy's Naval Sea Systems Command and General Dynamics for DDG 115's long-lead time material. General Dynamics' Bath Iron Works division is slated to fulfill the contract in Cincinnati, Ohio; Charlottesville, Virginia; Indianapolis, Indiana; Bath, Maine; Walpole, Massachusetts; Erie, Pennsylvania; and other locales by December 2012. DDG 115 is part of the DDG 51 class destroyer program, led by the guided missile destroyer USS Arleigh Burke (Figure 5).

Figure 5 | The guided missile destroyer USS Arleigh Burke is the lead ship in the DDG 51 class of guided missile destroyers. U.S. Navy photo by Paul Farley.

U.S. Air Force photo by Staff Sgt. Jacob N. Bailey

Static analysis improves efficiency, reduces downstream integration costs

By Andy Chou

With modern military systems increasingly relying on software, new techniques are being adopted to decrease costs and increase the chances for mission success. As a result, static analysis has been gaining traction in the software development community based on its deep analysis capabilities before runtime. These static analysis tools – which augment but do not replace traditional test and debug methods – find integration errors long before integration occurs, eliminating costly late-stage integration issues.

As military equipment and vehicles become increasingly modernized, they inevitably become more technologically complicated as well. In many instances, these machines represent a delicate blend of hardware and software, both of which must interact perfectly. Since the software components of these machines must work as reliably as possible in the field, it is important to perform extensive debugging and testing using a combination of techniques to eliminate defects before they cause extended delays or overruns. This is often impractical since there is usually no way to reliably test code until it is actually implemented into the equipment on which it will eventually run. Since software seldom works perfectly the first time it is executed, going back and fixing errors with conventional development methods and tools hinders productivity and diverts valuable resources and personnel from other projects that need to be completed.

For instance, the Boeing 787 Dreamliner was delayed for two years because of a combination of hardware and software defects. Often, such problems are intertwined; in the case of the Dreamliner, one particular delay was the result of defects in the software that controlled the braking system. It is important to note that conventional testing did not reveal this defect before it actually became a problem and caused costly setbacks and other complications in the development process. Modern techniques like static analysis can increase the probability of problems like memory corruption and user-after-free being discovered sooner, as well as assist in achieving DO-178B's Design Assurance Levels (DALs). A more efficient and cost-effective path than the traditional V-model, static analysis works in concert with traditional test and debug methods to ease integration woes and expense.

Static analysis and the development process

Software development tends to follow a specific life cycle. One example is the V-model (Figure 1), which is commonly

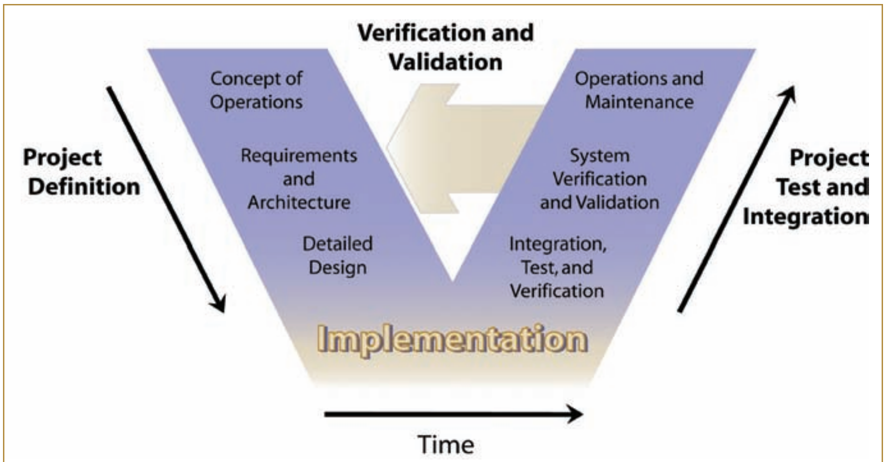

Figure 1 | The V-model represents a holistic approach to development that attempts to reconcile project definition and the testing process over a period of time.

used in aerospace engineering. The V-model represents a holistic approach to development that attempts to reconcile project definition and the testing process over a period of time. The model begins with establishing the scope of a project, including its concepts of operation, its requirements and architecture, and the specific details of its design.

This process starts out very abstract at higher levels and becomes gradually refined and detailed over the course of the design process. As the design is implemented, it becomes more expensive to fix problems later in the development cycle. Once the project is mostly complete and is being tested, going back and making repairs to its fundamental aspects becomes prohibitively expensive.

Ultimately, many software problems are caused and then worsened by an inefficient development model and imprecise debugging procedures. Development efficiency and cost-effectiveness can be improved by eliminating software defects as early as possible with modern techniques like static analysis.

Specifically, static analysis is a technique for finding defects in software without running it. It works by examining product source code, starting from individual functions, working its way up to modules, then ultimately the entire program. Static analysis can find many different kinds of defects, including memory errors in C/C++ programs. For example, static analysis can detect an error in this simple code fragment:

```
int a[10];
   for(int i = 0; i < 10; i++); {
      a[i] = 0;
   }
```

Sometimes it is hard for human beings to see problems in software code because they see what they want to see instead of what is actually there. When this code is turned into an executable program by a compiler, the compiler reads the source code in a mechanical and precise way, ignoring human cues like indentation and spacing. A compiler will read the example in the following way:

```
int a[10];
   for(int i = 0; i < 10; i++)
;
{
      a[i] = 0;
   }
```

Once the code has been reformatted as shown, an extra ";" character that causes the program to have a completely different meaning suddenly becomes much more visible. If this error remains uncorrected in the final program, the array access a[i] will execute only once when i = 10. The result is an assignment to a memory location past the end of the array, which might cause the program to crash.

Static analysis examines the code as mechanically and precisely as a compiler would. However, instead of blindly translating the code into an executable program, a static analyzer looks for paths where the code's function diverges from how the developer originally intended it to work. Static analysis can be done by techniques as simple as pattern matching or as advanced as interprocedural dataflow analysis and Boolean satisfiability. Regardless of technique, static analysis is custom-built to look for cases that human developers are likely to overlook or get wrong. This presents a far more efficient alternative to comprehensive line-by-line code auditing, which is not cost-effective for larger software systems.

Combine static analysis and traditional debugging

Compared with a traditional method such as functional testing, static analysis presents a different set of trade-offs. Traditional testing can only detect errors in code that is actually tested, whereas static analysis can find defects in all code without any tests. Sometimes, errors found through testing are hard to reproduce and pinpoint to a specific problem in the source code. Static analysis can find problems in a repeatable, predictable fashion and will always point to a specific location in the code. On the other hand, traditional testing can find functionality errors that static analysis cannot, because static analysis does not attempt to compare the behavior of the program against an expected result. Static analysis can also lose precision when analyzing deep program properties, so it might miss some defects. Therefore, static analysis is meant to augment the effectiveness of traditional methods instead of replacing them outright.

"Instead of blindly translating the code into an executable program, a static analyzer looks for paths where the code's function diverges from how the developer originally intended it to work."

Since static analysis works with existing toolsets and compilers, there is no need to change current development practices. Static analysis can be applied frequently

(even on nightly builds) for the duration of the project starting immediately after the first line of code has been written. Essentially, if the project's code base can be successfully compiled, static analysis can be used to debug it and eliminate problems long before the project is delivered to quality assurance personnel for final testing.

Integration benefits of static analysis

Static analysis also works well in a team-oriented environment. Developers can use static analysis to check each other's contributions for consistency and check for conflicts caused by code written by different team members. This can work within a single project or even scale to larger scenarios where integration between several projects is required to create a complicated system.

Static analysis can also do more than find simple code defects; as mentioned, it is capable of analyzing the interactions between different components before they are integrated together. In the V-model of software development, testing and verification start with individual components. When these components meet their low-level specifications, they are integrated together for higher-level testing against system requirements. If software integration is performed strictly according to this ideal, the integration phase introduces a high degree of risk because the individual components will be interacting for the first time. These interactions are likely to expose problems with the original project specifications, particularly regarding how the system requirements and architecture are translated into detailed design requirements and source code. Static analysis tools can analyze the interactions between software components as soon as they are written, catching some of these expensive integration problems during the implementation phase. The tools accomplish this by finding problems in Application Programming Interface (API) usage by analyzing code across procedure boundaries even if the procedures are in different software components.

Maximizing efficiency with static analysis

Software is being used to improve military systems such as smart bombs and unmanned drones in ways that were once impossible. Static analysis tools, such as those offered by Coverity, are also a part of this trend. Static analysis tools – when combined with traditional test and debug methods – effectively analyze software and detect code errors before runtime, minimizing risks and costs while maximizing the value of investment in software development.

***Andy Chou** is chief scientist and cofounder of Coverity. He is responsible for advancing source code analysis technology as well as furthering the state-of-the-art in software quality and security industry-wide. He received his Ph.D. in Computer Science from Stanford University and his B.S. in Electrical Engineering from UC Berkeley. He can be contacted at achou@coverity.com.*

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CFD simulations lower risk, pick up the pace of chassis design

By Drew Castle

Computational Fluid Dynamics (CFD) software has seen major advances in the past two decades. In the design of custom computer chassis for mission-critical components, CFD software simulations allow accurate determination of the performance of cooling components, clarifying how specific configurations perform, thus cutting design costs and risks and increasing the speed at which concepts become products.

A thermometer measures the temperature of a newly-paved road in Mahmood Rahqi, Afghanistan, Sept. 9, 2009. The temperature registers 137 degrees Fahrenheit. The optimal temperature is between 135 and 150 degrees Fahrenheit. U.S. Army photo by Sgt. Teddy Wade

In computer chassis design, many basic needs can be tailored to motherboard, processor speed, communication, storage requirements, and size limitations by simply putting the correct off-the-shelf components into an appropriately shaped box. However, one integral design consideration that simply cannot yet be ignored or handled as a quick matter of routine (no matter how advanced the rest of the components are) is the cooling of the chassis. A simple temperature elevation in a poorly designed chassis can cripple even the fastest and most robust systems. And this becomes increasingly critical in the design of custom systems, where "off-the-shelf" is a four-letter word.

The new mantra in computer performance is: "More stuff – More power – Small box." When these systems are required to function in ambient temperatures exceeding 100 °F and people are counting on them for necessary information, the stakes get even higher for effectively designed systems. Ruggedized chassis designed for use in the current battlefield environment are subjected to extreme conditions every day. There is no tolerance for failure and design, and production deadlines must be kept.

As a result, CFD simulation software has become an increasingly used tool as both programming and processor capabilities have become more advanced and refined. The software allows a set of conditions to be applied to an existing three-dimensional model. Then the software calculates resulting flow characteristics, thermal profile, and overall chassis cooling. Complicated Navier-Stokes equations describing the flow field of fluid – once shrugged off by engineers in favor of a best-guess or tried-and-true design dogma approach to engineering – are now embedded in software readily available to any engineer. The advantages:

"A simple temperature elevation in a poorly designed chassis can cripple even the fastest and most robust systems. And this becomes increasingly critical in the design of custom systems, where "off-the-shelf" is a four-letter word."

nearly instant access to answers to the cooling equation, plus the ability to monitor the effects of design changes throughout the design process rather than trying to fix underlying problems after a product has been designed, built, and evaluated. The result: design time reduction.

How CFD simulations work

CFD simulations operate by a method of Finite Element Analysis (FEA). In FEA, a control volume of solid, liquid, or gas is broken down into cells defined by a mesh grid. In the case of CFD, calculations of heat transfer through various media and fluid dynamics of the flowing air are done on a cell-wise basis, with each cell in the mesh grid influencing the other cells surrounding it. With detailed components, it is possible to optimize the mesh in a manner that provides smaller cells with more refinement around these components rather than in large spaces with bulk conditions.

Setting up a simulation with the aforementioned points in mind becomes a bit of an art. Developers determine how specific to make the mesh in certain regions of a model while negating this specificity in other regions while still extracting accurate results. In full simulations on complex chassis, it is not uncommon to create meshes comprised of more than half a million cells.

As with any tool, the quality of CFD results that can be achieved by a craftsman versus those achieved by a novice are a function of experience. Thankfully, CFD software developers are increasing the usability of their products to constantly accelerate that learning curve and help novice users quickly arrive at accurate results. An example illustrates the benefits and innerworkings of CFD.

Example: CFD simulation

The operations and advantages of CFD software can be seen through a simple exercise of varying the installation of a fan in a computer chassis. To simplify the images, the temperature field through the chassis has been hidden on the representative graphics herein, but it is important to know that CFD can determine the heat transfer as well as the flow field.

Many designers, when it comes to solving internal temperature issues, simply place enormous fans directly in front of important components, believing that increased air velocity is sufficient for cooling. While the increased velocity does have a cooling effect, it quickly wears off if the heated air is allowed to remain in the chassis. In Figure 1, a simplified chassis with one large 120 mm diameter internal fan, capable of pushing 120 cubic feet of air per minute (CFM), has been modeled in two chassis configurations to show airflow through the chassis. The streamlines in the two pictures in Figure 1 show the actual path of air throughout a three-dimensional chassis rendering.

The left side of Figure 1 shows a typical design with an open bulkhead positioned mid chassis with the fan mounted to the bulkhead. As depicted, often a large area is left open to allow for easier routing of cables past the bulkhead. This is a common design element in low-end chassis built for consumers with basic needs operating in simple environmental conditions. In this simplified instance, there are minimal accessories in the chassis so the airflow is clearly visible. The only actual cooling airflow is represented by the streamlines shown entering the front of the chassis from the left side of the image, and exiting via the opposite wall. As this particular simulation was performed as an analysis of internal flow conditions, streamline behaviors after exiting the chassis were not calculated, and therefore do not appear in the diagram.

While the internal fan increases the air velocity in the chassis, the ability to transfer heat from the solid surfaces to the moving air is dramatically reduced as the temperature of the recirculating air increases. This is a key consideration in determining the resultant thermal profile of the chassis. While the empty chassis

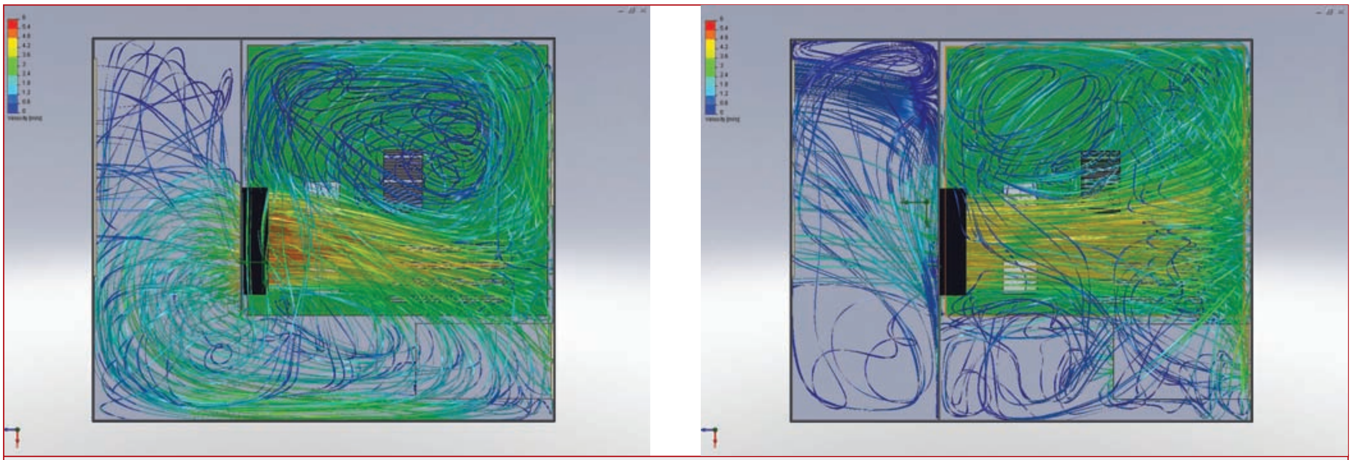

Figure 1 | An unsealed chassis bulkhead (left) compared with a sealed bulkhead (right) shows a net airflow improvement of 184%, a simple calculation using CFD software.

allowed the fan to push 112 CFM, the actual net airflow through the chassis was a mere 37 CFM. Once the chassis was sealed, though, as shown on the right side of Figure 1, the airflow rose to a much more respectable and effective 105 CFM through the chassis. The placement and design concessions made for cooling fan installation should not be an afterthought, but amongst the most important initial design concerns. While some internal fans are necessary to direct much-needed air to sensitive components buried within a labyrinth of wiring and circuitry, their implementation must be well thought out and tested before modifying designs to accommodate them.

The simple analysis offered by CFD software shows us not only the actual path air takes as it moves through the chassis, but also calculates for us the exact volume of air entering and exiting the chassis through each vent over time. While it is possible to predict streamline behavior based on a "common sense" design approach, accurately measuring the volumetric airflow through a chassis by experimental methods is a much more complicated and time-intensive process than utilizing CFD software. If we were to choose to pursue that method of design, it wouldn't be until a fully assembled chassis were drafted, built, and bench-tested that we would discover the disparity between fan capability and the actual net flow rate. At that point the options would be a redesign of the entire product, or making last-minute concessions to improve the existing faults. Having this information available early in the design process allows design modification to achieve optimum performance.

CFD simulations: The result

In designing custom chassis for extreme environments, CFD simulations are often useful in saving time and helping verify configuration changes throughout the design process. Figure 2 shows a fully configured 4U chassis designed by Chassis Plans and similar to one used in Iraq and Afghanistan. Its redundant power supplies, multiple SBCs, CPU coolers, and inlet fans modeled for CFD analysis serve as an example of a chassis where the interaction between design geometry and fan performance is difficult to predict with so many different elements.

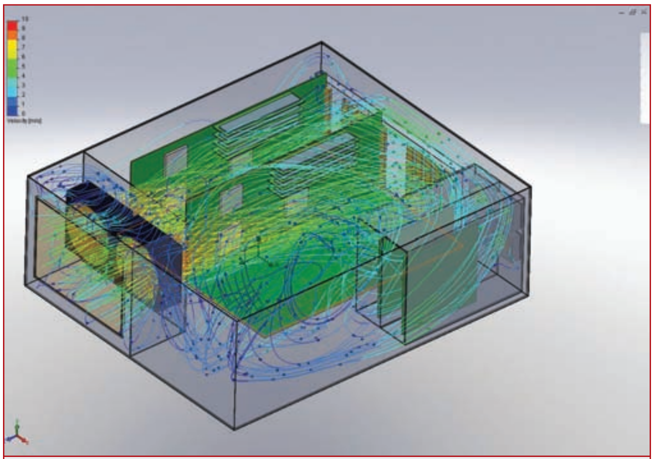

Figure 2 | A more complex chassis with multiple flow variables is still a simple matter for CFD software simulations and analysis.

Though moderate simplification was done on this model to improve calculation times of the software, the calculation results still maintain a high degree of accuracy. The large inlet fans push air through the chassis, across sensitive components on the SBC, while smaller fans in the power supplies direct air over the heat-generating components of the power supplies. Meanwhile, CFD allows accurate visualization of flow trajectories, giving a clear picture of how this configuration performs in extreme conditions before engineers turn even one screw.

***Drew Castle** is a mechanical and thermal design engineer at Chassis Plans. His career spans a decade of varied positions in the high tech industry. He is currently pursuing a graduate degree in mechanical engineering with a thermal sciences specialization. He can be contacted at drewc@chassisplans.com.*

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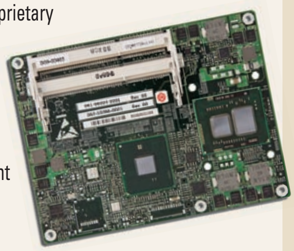
Intel Core i7/i5 Product Spotlights

RadiSys THE POWER OF WE

The Procelerant™ CEQM57XT module combines the Intel® Core™ i7 and i5 processors and the Mobile Intel® QM57 Express chipset with extended temperature range from -25 to 70 °C and ruggedized vibration specifications that are required for many mil/aero and industrial applications such as ruggedized computers/tablets, unmanned vehicles/robots and in-vehicle computers. RadiSys designs ruggedness into the CEQM57XT by utilizing its proprietary implementation of the Highly Accelerated Life Test (HALT) during the design process to identify and correct product weaknesses prior to production; Highly Accelerated Sample Screen (HASS) is then used during production to continually monitor supplier quality and component robustness.



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SPECIAL ADVERTISING SECTION

MIL/COTS DIGEST

The Defense Electronic Product Source

March/April 2010

In This Issue

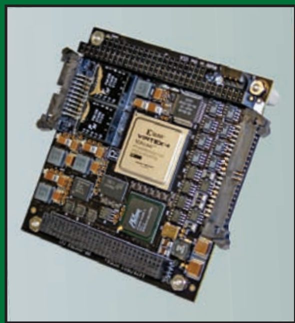
SFFs band together to face the battlefield

First-person shooter games aside, modern warfare involves an array of advanced technologies working in tandem to provide the greatest performance with the highest reliability, a difficult feat in harsh, space-constrained environments. Small Form Factor (SFF) boards, which are finding increasing acceptance in defense applications, must support and enhance a variety of embedded products, from touch screens to mission computers to software, as part of a cohesive, interconnected COTS military system.

This edition of *MIL/COTS DIGEST* highlights rugged SFF products specifically designed to meet military specifications for extended temperature, humidity, EMI, and other challenges typical of defense applications. These compact modules, including an ARM9 RISC computer, video encode/decode PMC card, and MIL-STD-1553A/B PC/104-*Plus* board, offer low-power operation and flexible programmability. Ethernet cards including a GbE switch card and family of LAN modules likewise provide numerous I/O options and connectivity, while a PCI/104-Express serial board enables expansion from legacy PCI-104 cards to PCI Express stacks. And, as an integral part of any SFF system, a software board support package facilitates the development of LabVIEW applications for MIL-STD-1553 and ARINC 429 hardware.

In addition to these rugged SFF products, this issue of *MIL/COTS DIGEST,* compiled in association with our sister publication *PC/104 and Small Form Factors*, features two articles covering the topic of rugged gear for today's battlefield. Parvus examines a military-grade flight display system built on a PC/104-*Plus* platform while Ampro ADLINK Technology discusses the benefits of using EFI BIOS in SFF designs for extreme rugged applications. Both articles emphasize the importance of rigorous design throughout an entire system, from the smallest hardware components to the software running the program.

Chris A. Ciufo, Group Editorial Director



Flight-ready PC/104-*Plus*

The PC104p-1553 is a rugged, full-featured PC/104-*Plus* module with up to two dual-redundant MIL-STD-1553A/B data bus streams, providing a flight-ready MIL-STD-1553A/B interface for avionics applications. Using a high-performance FPGA-based hardware architecture, the module includes six fully programmable discrete I/O lines and 128 MB of DDR2 SDRAM to handle high volumes of data and complex simulations. Each MIL-STD-1553A/B channel can be configured to simulate a bus controller, bus monitor, or 31 remote terminals. Offering an IRIG-B time code decoder for common time source synchronization and a -40 °C to +85 °C extended temperature range, the PC104p-1553 comes with AIM-USA's MIL-STD-1553 Object Wrapper Layer (OWL) C and C++ interface library for intuitive, object-oriented interfacing to the module. Software drivers for Windows, Linux, and various RTOSs (VxWorks, Integrity, LynxOS) are available.

www.aimusa-online.com **AIM-USA**

High-def MPEG-4 PMC

The PMC-281 is a rugged MPEG-4/H.264 high-definition video capture/compression PMC interface card that uses an ASIC for low-power compression, making it suitable for deployment in harsh environments such as naval, jet, helicopter, and UAV platforms. Using the H.264 baseline and main profile up to L4.2 (MPEG-4 Part 10/AVC), the card provides real-time compression of resolutions up to 1920x1200 pixels. Available configurations include one channel of 1080p60 encode/decode or two channels of simultaneous encode/decode at resolutions up to 1080p30/1080i60. Each I/O can be selected from digital DVI, analog RGB, or PAL/NTSC composite. Captured video can be compressed or transmitted via a 33 MHz, 32-bit PCI interface. Offering less than 12 W power dissipation, the flexible PMC card is available with a -40 °C to +85 °C operating temperature.

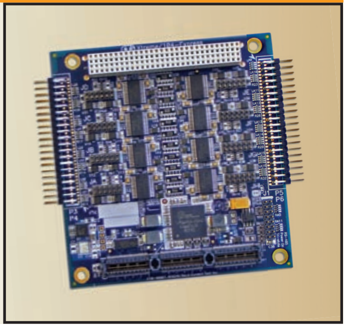
www.cwcembedded.com
CURTISS-WRIGHT CONTROLS EMBEDDED COMPUTING

Rugged GbE switch card

The COM-1268 is a rugged PC/104-*Plus* GbE switch card with 10 triple-speed 10/100/1000 Mbps ports for connecting IPv4 and IPv6 devices. Designed to meet MIL-STD-810G specifications for -40 °C to +85 °C operating temperature and up to 95 percent humidity tolerance, this SFF Layer 2 switch provides enhanced situational awareness and IP net-centricity in space-constrained military applications. An RS-232 console is available for Command Line Interface (CLI) management, status LEDs, and zeroization. Featuring an onboard microprocessor for local/remote monitoring, the card offers support for Quality of Service (QoS) traffic prioritization, Virtual LAN (VLAN) trunking, Simple Network Management Protocol (SNMP), and Rapid Spanning Tree (RSPT) redundancy. The COM-1268 can be used alone or integrated into a military-hardened enclosed switch subsystem, mobile router subsystem, or mission computer platform.

www.parvus.com **PARVUS CORPORATION**

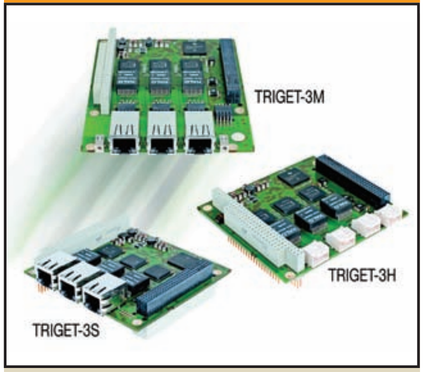
Robust 8-port serial board



The Xtreme/104-Express is a PCI/104-Express RS-232/422/485 add-in card with rugged filtering on all ports for immunity to EMI and noise. With a PCI-104 connector for transitioning from legacy PCI-104 cards to PCI Express stacks, the board offers eight serial ports up to 15.625 Mbps and 9-bit data support with 128-byte FIFOs per port. In addition to fail-safe transceivers, the Xtreme/104-Express incorporates -40 °C to +85 °C operating temperature-grade components to withstand harsh environments.

www.connecttech.com
CONNECT TECH, INC.

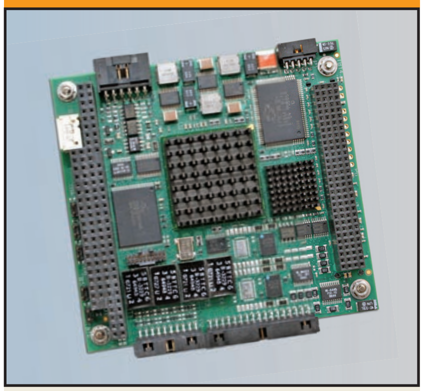
Triple Ethernet modules



The TRIGET family consists of robust PC/104-*Plus* LAN modules that enable system expansion with up to three rugged GbE controllers. Using a PCI-to-PCI bridge, each module requires only one PC/104-*Plus* slot, allowing up to three more PC/104-*Plus* boards to be added to the stack. The modules offer 33 MHz/66 MHz PCI operation and support both 5 V and 3.3 V signaling. A -40 °C to +85 °C extended temperature version is available.

www.mpl.ch **MPL AG**

MIL-STD LabVIEW BSP



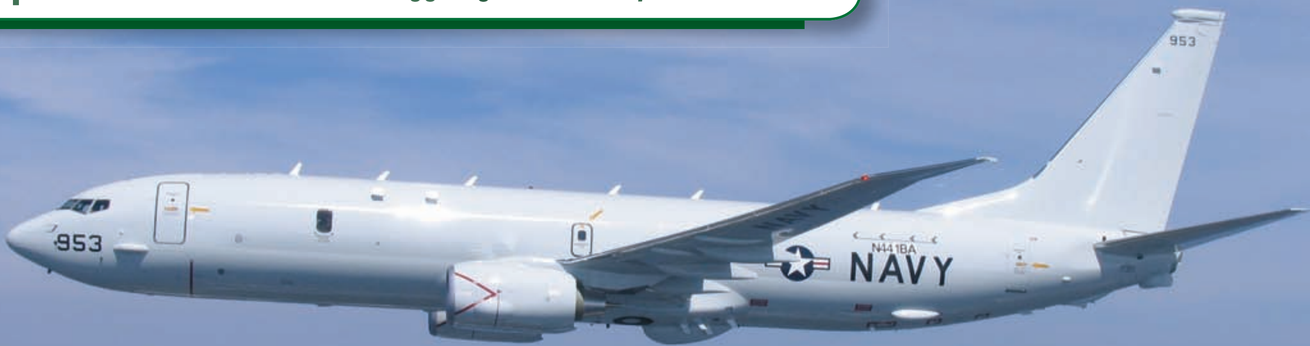
The BU-69093 LabVIEW Support Package enables the development of LabVIEW applications for DDC's MIL-STD-1553 and ARINC 429 hardware, including the BU-65590C rugged multiprotocol PC/104-*Plus* card (pictured). The package provides all the necessary Virtual Instruments (VIs) to develop a versatile LabVIEW application, including fully functioning front-panel user samples, block diagrams, and connector panels. Features include an intermediate-level VI interface for quick startup and a set of low-level VIs for advanced functionality and customization in unique applications.

www.ddc-web.com
DATA DEVICE CORPORATION

Compact ARM9 computer

The Relio R9 is an ARM9 embedded RISC computer housed in a compact, rugged enclosure rated to a -40 °C to +85 °C operating temperature range. Based on the 200 MIPS Atmel AT91SAM9263 microcontroller with a 32-bit ARM instruction set, the platform offers up to 256 MB RAM and 256 MB flash memory plus a high-level, object-oriented .NET Compact Framework interface. In addition to standard I/O, the system supports LCD and resistive touch-screen controllers.

www.sealevel.com **SEALEVEL SYSTEMS**



Arming the latest anti-submarine aircraft with COTS multifunction displays

By Dave Turner

*Modern military aircraft demand display panels that fulfill rigorous standards for flight certification and enable expansion for future requirements. This case study examines how engineers designed a military-grade display system built around a modular PC/104-**Plus** platform.*

Ruggedizing Poseidon for the future battle space

Boeing's latest military derivative aircraft, the P-8A Poseidon, is a testament to the technical innovation taking place in military aircraft design. Capable of broad-area maritime and littoral operations, the P-8A will influence how the U.S. Navy's maritime patrol and reconnaissance forces train, operate, and deploy.

Ensuring the success of the P-8A's mission requires tracking the operation of various electrical components inside the aircraft. To help pilots with this task, test display panels are placed inside the cockpit to inform both the pilot and copilot about how these subsystems are functioning as the new platform undergoes flight qualification. Because of stringent Navy avionics requirements and various military standards, these flight display panels must be ruggedized to guarantee optimal performance.

Combining computing power and display functions

To build these cockpit display systems (shown in Figure 1), Boeing collaborated with Parvus Corporation to provide the Flight Test Display (FTD) and the Instrumentation Crew station Control Panel (ICCP) for the P-8A Poseidon aircraft. The project also involved designing a custom DVGA switch to simultaneously display the data on both of the cockpit FTDs. Boeing selected these displays because they allowed engineers to leverage existing COTS hardware that was hardened to the operational parameters expected to take place during the Poseidon's flight testing. A Dzus rail-mount panel and set of flip-down display-mounting brackets were configured for these COTS designs.

Parvus engineers set about the task of developing the ICCP by combining the proven durability and power of the company's DuraCOR mission computer with its legacy COTS Multi-Function Display (MFD). The ICCP later became the DuraVIS 4300, a new MFD for presenting flight, sensor, mapping, advisory, and other information to the crew.

Figure 1 | The P-8A Poseidon cockpit uses test display panels from Parvus Corporation to track the operation of various electrical components inside the aircraft. (Photo courtesy of Boeing.)

> “Engineers designed each subassembly with a pressure differential per a robust set of rules, including a safety margin of 200 percent, to maintain structural integrity ...”

Overcoming EMI roadblocks

As work began on the ICCP, engineers quickly learned that ruggedizing these displays to meet the Navy’s exacting requirements for flight certification required creative engineering. For example, the displays created some difficulties with EMI that initially prevented the system from passing certification tests. MIL-STD-461E test parameters required compliance with CE101, CE102, CS114, RS101, RS102, and RS103 requirements for conducted and radiated emissions and susceptibility across various wavelengths and frequencies. To alleviate this issue, engineers worked with a manufacturer that produced a specialized indium tin oxide material to develop a coating that would provide the right level of clarity and brightness while preventing electrons from entering or escaping the displays. The coating they developed immediately passed testing without presenting any additional EMI issues.

The end result was a robust, flight-qualified mission computer that included an integrated, sunlight-readable 6.5" LCD screen equipped with an anti-glare cover for impact protection and a high-luminance (800-nit) LED backlight for long lamp life and dimming capabilities.

Modularity ensures longevity

The unit needed to undergo rigorous MIL-STD environmental and EMI qualification testing and be based on open architecture embedded hardware. In addition, Boeing wanted the ability to add PC/104-*Plus* I/O boards into the subsystem’s card slots to meet future mission requirements. Consequently, options for MIL-STD-1553/ARINC 429 bus controllers, digital I/O interfaces, synchronous/asynchronous serial controllers, and video capture devices were included in the system design. A 79-pin expansion connector on the rear panel was routed to an internal breakout board and headers to support application-specific PC/104-*Plus* card integration without mechanical changes.

Ruggedizing to the highest standards

Because the P-8A Poseidon is a long-range intelligence, surveillance, and reconnaissance aircraft intended for anti-submarine and anti-surface warfare, the embedded designs within the aircraft had to endure extreme testing and engineering revamps to ensure the highest-quality rugged platform for the Navy. Furthermore, the aircraft presented specific ruggedization challenges, such as altitude requirements, temperature variations, vibration, and crash safety. Equipment inside the P-8A is in a pressurized environment but must survive decompression to altitudes between 30,000 and 40,000 feet.

To ensure the system’s ability to operate in a pressurized environment, engineers utilized designs and testing results from previous projects and applied this knowledge and experience to the new unit. Engineers designed each subassembly with a pressure differential per a robust set of rules, including a safety margin of 200 percent, to maintain structural integrity even in the event of a sudden change in pressure. Consequently, no issues with pressurization or rapid decompression were presented during qualification testing per MIL-STD-810F (Method 500.4, Procedure 3) from 1,500 feet below sea level to 41,000 feet above.

In addition, the unit needed to survive crash safety parameters to ensure that no portion of the display or MFD would create a hazard to personnel. All metal work, fasteners, and mechanical design considerations targeted high reliability and flight safety. Several components were bonded to the printed circuit boards. Certain cables were removed and cable lengths were restricted to eliminate wire breakage under stress. Again, the system passed qualification testing with no changes required. In fact, the unit survived the crash safety tests in a fully functional state.

Thermal management often presents a challenge for embedded designs within aircraft, as fewer air molecules are available to dissipate heat at high altitudes. At 40,000 feet, roughly one-fifth of the amount of atmospheric pressure (2.7 PSI) is available for convective or conductive cooling compared to at sea level (14.7 PSI). By physically oversizing heat sinks, performing calculations at the higher pressure differential, and conducting initial thermal evaluation tests in-house before full MIL qualification testing, engineers ensured that the system would perform well in a high-altitude environment. Test results confirmed that the system would meet the targeted -20 °C to +60 °C operating temperature range and -55 °C to +71 °C storage temperature range.

In the end, the DuraVIS 4300 (Figure 2) passed all required standards, including MIL-STD-810F, MIL-STD-704E, and MIL-STD-461E. Additionally, although destined for installation in a crew environment, the equipment was tested using the shock and vibration conditions present in other rough locations. The P-8A's flight display systems were tested to the same shock (15 *g* sawtooth) and random vibration profiles (0.022 g^2/10 Hz to 0.0026 g^2/2,000 Hz) that would be required if they were moved to harsher environments, ensuring the highest standard of ruggedized durability. This robust system design philosophy has led to follow-on projects with single- and multi-core processors onboard the AC-130, CP-140, and P-3.

Figure 2 | The Parvus DuraVIS 4300 and 3006 display systems are used inside the Boeing P-8A Poseidon aircraft.

Creating a flight display system that can withstand environmental challenges to meet the Navy's stringent requirements while still being usable for pilots requires creative engineering to surmount difficult design parameters. Installing rugged PC/104-based systems such as the DuraVIS 4300 in a prestigious aircraft like the P-8A Poseidon provides the necessary equipment to ensure maximum interoperability in the future battle space.

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EFI BIOS brings new capabilities and robustness to rugged SFF designs

By Qi Chen, PhD

Building robust systems requires ruggedness to be designed into the firmware and software, not just the hardware. Qi discusses the advantages of using EFI BIOS in small form factor designs for extreme rugged high-reliability applications such as military systems.

Extensible Firmware Interface (EFI) provides the current direction for the BIOS functionality needed in embedded systems. New EFI-based solutions can be used to make rugged embedded applications significantly more robust, secure, and reliable.

The following discussion focuses on embedded EFI BIOS, pre-boot applications, interfacing to custom hardware using EFI drivers, and EFI's ability to provide the Small Form Factor (SFF) market with an enhanced rugged embedded solution for critical applications.

EFI history

Dating from the late 1990s, EFI is an Intel development aimed at replacing the traditional BIOS that has been present on PC architecture systems and embedded motherboards from the beginning of their history. EFI is therefore already a significant development for the embedded systems industry because of the prevalence of the BIOS it aims to replace.

EFI provides a more straightforward method for interfacing user applications to hardware functions on the motherboard compared to the complex and unwieldy mechanisms typically needed in traditional and current non-EFI BIOS implementations.

Rugged by design

Because failure is not an option in rugged embedded systems, rugged embedded design philosophy must include the most robust and reliable approaches to avoid failure.

Achieving robustness is not just about using high-reliability hardware that can survive extremes of temperature and shock and vibration; it also applies to the software and firmware within the system, which must behave reliably and predictably in all situations. Ruggedness in hardware is achieved by using the highest-quality components and implementing the most careful and rigorous design approaches with no compromises. In short, ruggedness must be designed into the hardware product.

Firmware and software robustness is likewise achieved by design. Only the most well-proven software elements should be used. This is where EFI offers significant advantages over traditional *ad hoc* BIOS approaches, providing custom hardware with established interface capabilities for user software applications. Complex low-level interfaces to hardware are handled by proven EFI drivers, ensuring implementation reliability.

Many extreme rugged SFF systems include complex hardware features that must be accessible by the user application. EFI drivers offer a suitable solution for interfacing this underlying hardware to the user application that controls such a system.

Benefits of pre-boot applications

A pre-boot application typically runs after all power-on self-test and diagnostics have completed and before the OS loader runs to boot the OS. See the time flow shown in Figure 1.

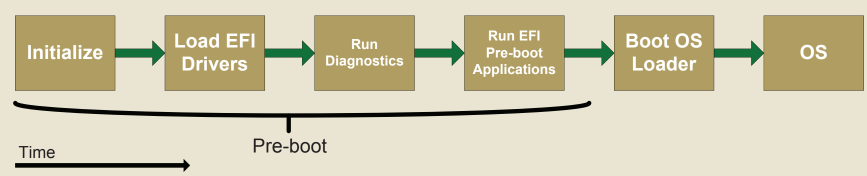

Figure 1 | The EFI BIOS boot process enables pre-boot applications that can perform security and configuration tasks outside the OS environment.

Using a pre-boot application allows specific customer actions to be performed using customer code before the OS boots. The EFI environment provides a proven pre-boot shell that customers can use to develop and run their EFI pre-boot applications, such as setup, OS installation, diagnostic, or configuration utilities.

Specific examples of pre-boot applications include checking the file system on the disk for the presence of certain files, verifying if sufficient storage space is available, confirming that the necessary peripheral devices are present and functioning, implementing special security features, encryption and de-encryption routines, data integrity verification prior to boot, automated device configuration, and user selection of bootup device options prior to boot. With EFI, all of these functions can be completed prior to OS boot by customer code using high-level API interfaces in C instead of rewriting complex low-level BIOS code. Thus, EFI pre-boot applications are often used to check the boot environment by customer code before the OS boots, which is easier than using traditional BIOS approaches.

Other areas where pre-boot applications are helpful include hardware diagnostics (for example, checking if a hard disk device is connected and functioning correctly), testing and verification of custom hardware functionality prior to booting the OS, OS selection and installation, and other security and configuration tasks that need to be performed outside the OS environment. Using EFI, pre-boot applications can achieve higher levels of system reliability and control than what was previously possible.

Running without an OS

EFI also enables custom systems to run user applications in a non-OS environment. Instead of booting to the OS, the EFI runs a user application directly. This approach does not match the needs of all customers, as some applications require the complexity and multitasking capability an OS provides. But for some developers working with applications that are well-developed, stable, and do not make extensive OS calls, the possibility of not needing an OS can be attractive for multiple reasons. These include design robustness due to the removal of the complex OS, extra storage space that would have been consumed by the OS, lower cost, and faster execution.

User applications running directly from EFI provide the fastest possible boot time and are suitable for systems that implement a dedicated function. Execution speed and interrupt response times can be made fast and predictable in a non-OS environment.

Another advantage to running an application directly from EFI is enhanced security, given that the security weaknesses of a complex OS are not present and the developer has control of all operations performed by the system. These are important requirements for rugged systems developers who must provide the highest levels of robustness and reliability.

Accessing SPI flash via EFI drivers

To demonstrate the capabilities of EFI drivers, consider the latest Intel Calpella platform and Ibex Peak chipset with support for Serial Peripheral Interface (SPI) flash, which can hold data space in addition to the firmware code space traditionally stored in flash.

For embedded systems, SPI flash is typically used to conveniently store system configuration information and status in a reliable storage area. This data space is accessible to the user application, but accessing the space to retrieve or update the data can introduce significant code complexity, thereby lowering reliability. Furthermore, implementing SPI flash access within the user application means that the SPI interface cannot be fully verified during the development phase or when the system is deployed, which is another disadvantage for achieving high reliability.

SPI flash is accessed over a 4-wire interface consisting of clock, data input and output, and chip select. Controlling this hardware directly requires in-depth knowledge of the interface, timing, and protocols; thus, using a dedicated SPI driver to manage the interface is a more satisfactory solution than implementing SPI flash in the user application.

EFI provides a simple solution for this by tasking the EFI drivers with handling the complexity of driving the SPI interface and accessing the appropriate address space for the platform data. EFI thereby provides the SPI device with a higher-level interface in the form of an API for the user application. This gives user applications a straightforward way to access the platform data area by calling the EFI driver to read and write to the platform data region in SPI flash.

This is an important benefit because it lets companies manufacturing complex, full-featured embedded systems offer high-level user applications easy access to these features through proven EFI drivers. The drivers can be exhaustively debugged and validated by the embedded system supplier and verified to behave correctly under all conditions.

Built-in software reliability

The Ampro by ADLINK Express-CBR COM Express module pictured in Figure 2 provides an example of an embedded design for applications that require ruggedness in both hardware and software/firmware.

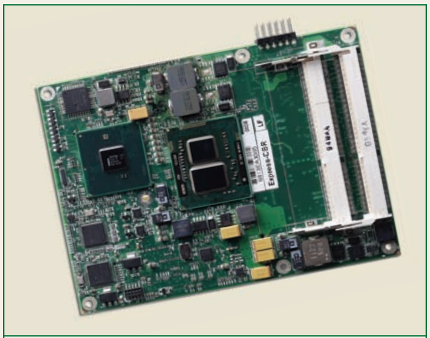

Figure 2 | The Ampro by ADLINK Express-CBR COM Express module uses EFI BIOS to improve software reliability.

Hardware ruggedness is achieved by component selection and an Extreme Rugged design methodology to enable reliable operation from -40 °C to +85 °C. On the firmware side, EFI is provided and enables the extra features and capabilities described earlier, such as pre-boot applications. EFI software drivers allow easy software access to the two SPI flash devices' separate storage spaces for program and data storage requirements. The software accesses the SPI flash storage using robust and verified drivers, thereby enhancing overall software reliability.

Systems based on EFI thus provide significant features for developing secure, extreme rugged embedded applications compared to those based on legacy BIOS implementations. For many application areas, EFI offers new and valuable capabilities that are relatively straightforward to implement. Because of the reasons discussed earlier, it is expected that EFI will become widely adopted in the embedded systems industry as the implementation of choice that might eventually replace BIOS altogether.

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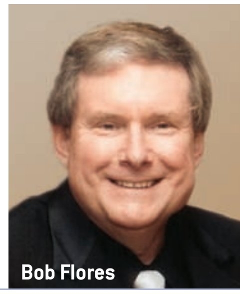
Cloud computing offloads legacy hardware, balances loads, and puts the focus *back* on the application

Interview with CIA veteran Bob Flores and Appistry founder Bob Lozano


Bob Flores


Bob Lozano

EDITOR'S NOTE

Though the precise technicality behind Internet-based "cloud computing" is not often understood, we've all heard of – and likely used – at least one of its incarnations: Google, Amazon, Yahoo, Facebook, or even SalesForce.com. However, you might be surprised to learn that the Defense Information Systems Agency (DISA)'s fiscal year 2011 budget estimate states that, "The President's FY 2010 budget emphasizes the trend towards cloud computing as a key tool for improving innovation, efficiency and effectiveness in Federal IT. The FY 2011 funding will continue … towards a more elastic computing, or cloud computing, environment." To explore this forthcoming DoD adoption of cloud computing, Editor Chris Ciufo recently interviewed Bob Flores, a 30-year CIA veteran and Bob Lozano, founder of Appistry, to explore the emerging trend. Edited excerpts follow.

MIL EMBEDDED: ***So I use simple cloud computing services such as salesforce.com, Google documents, or Dropbox, accessing them from my Internet browser while the actual application resides elsewhere and the "magic" just happens?***

LOZANO: Absolutely. How cloud computing works is that there's the infrastructure at the bottom layer, sometimes referred to as Infastructure as a Service or "IAAS." Then there's the cloud platform or "Platform as a Service" in the middle. And then there is "Software as a Service offering" or "SAS" at the top. All the examples you cited are Software as a Service offering.

> "An arbitrary number of computers can look like one computer to the application, so that developers don't have to do a lot of extra work as the application grows. This is accomplished again through cloud computing's capability to scale up and down or its 'elasticity.'"

MIL EMBEDDED: ***I assume Appistry provides the cloud platform in the three-layer model?***

LOZANO: That is correct. So as a platform provider, we make it very simple for anybody who wants to make their own Software as a Service offering.

MIL EMBEDDED: ***So can users use their own existing infrastructure?***

FLORES: Right. They can use their existing application layer and existing hardware layer, and they can stick Appistry in the middle of it. Appistry takes the applications and spreads them across the computing resources that are available. So users are not locked into a certain server. Through the management piece, users can also limit an application to certain servers if they want to.

MIL EMBEDDED: ***Is the infrastructure hardware typical rack-mount servers like you'd see in any ISP or in the Internet cloud?***

LOZANO: It can be. It can also include much more aggressive commodities from there. One way to think about it is an ISP. If it's primarily doing purely Web-based serving or Web-based technologies, then it will tend to be more consistent, for rack-mount 1U kinds of things. But in many cases they might have dialed it up for things like the database and that sort of thing. We would enable that to be rack-mount style or even more commoditized [platforms].

FLORES: [Appistry's SAS] can also be utilized on virtual servers, alleviating the need for homogeneous or expensive dedicated "iron."

MIL EMBEDDED: ***You're saying the Appistry SAS does a good job of abstracting legacy hardware and legacy applications and enables tech insertion and tech refresh. So could the Aegis control system, for instance, be taken from its existing infrastructure and ported to something different, or be spread across other pieces of Navy infrastructure?***

FLORES: Perhaps, it all depends on exactly how it was written.

LOZANO: At a high level, there's the infrastructure level out there that either comprises physical or virtual servers, as we mentioned. But another question that arises when, let's say, I have 10 or 100,000 of these servers is: How am I going to assure that they're all operating with consistent "fuel" for the applications?

Appistry handles this scenario via the Cloud IQ Manager, a hardware management platform. That way, the platform utilizes self-organization techniques, a lot of pretty advanced concepts so that the operator doesn't have to worry how many servers are operating, whether 10 or 100,000.

FLORES: And not only that, cloud computing is also known to be "elastic." To illustrate this concept, let's take something like a payroll application. If the payroll runs once a month, then when it's between run times, it might actually be up and running and processing tasks, but it's not doing its heavy computer-intensive executions and so it won't require the computer resources that it will when it's actually payroll time. In the past you didn't have any choice. You would have to say, "Well I have to account for surge, so I have to go buy a server or a bunch of servers that are big enough – or if I lash them together they'll result in a server that's big enough to handle the load when I surge on this payroll application that I'm processing."

MIL EMBEDDED: ***Meaning: You had to design to the worst common denominator.***

FLORES: That's right. But with cloud computing, you don't have to do that because the Appistry layer will help monitor the application by saying, in essence, "Oh you need more resources? No problem. I see some other resources out here. I can grab those resources and allocate them to you while you're doing your surge processing and then I'll release them."

MIL EMBEDDED: ***So the big benefits of cloud computing, then, are resource elasticity and resource loading such that you can bring additional processing on-the-fly?***

FLORES: Yeah, it's kind of both. In the past we'd say, "OK, well we know what's going to happen if the payroll needs to surge, we're going to need this kind of CPU resources" and, "Oh well, if the financial application needs to surge, then it needs this kind of resources available." And you basically had to add the two together; you could never rob Peter to pay Paul, but now you can. And so now maybe instead of having x+y, you only need to have x + half of y [processing resources].

MIL EMBEDDED: ***Is cloud computing reliable?***

LOZANO: Yes. Let's say you have a server that can be used for anything from simple Web applications to much more sophisticated distributed applications, things like next-generation applications and so on. Then for example, suppose you wanted to make those commodity processors more reliable. Using a platform layer, configured around our Cloud IQ Engine, many virtual or physical machines' infrastructures are "ganged" so that they all look like one compute resource and can back each other up.

That way, an arbitrary number of computers can look like one computer to the application, so that developers don't have to do a lot of extra work as the application grows. This is accomplished again through cloud computing's capability to scale up and down or, as mentioned before, its "elasticity." It means things like if you need it to be more reliable because maybe there are increased drop levels, then you can dial up the level of reliability provided. It will happen without a lot of manual interaction or programmatic work.

MIL EMBEDDED: ***So Mr. Flores, you're a CIA veteran. What is your perspective on all this from a government adoption standpoint?***

FLORES: I'm on Appistry's federal board of advisors as well as an independent member on their board of directors because they have a technology that I totally believe in. And it's vitally important for government entities – be they defense, intelligence, or other – to embrace cloud computing in a big way. For most government agencies that's going to mean private clouds, as opposed to public clouds, however.

MIL EMBEDDED: ***What are the drawbacks of that?***

FLORES: Obviously there is a whole host of reasons why a government agency might not want to have its data out in a public cloud, but government can still gain the economies of scale that the cloud offers by building their own private cloud. And when I say building their own, it doesn't necessarily mean that they take everything government has today and throw it out; it just means they would use it more efficiently.

MIL EMBEDDED: ***What are the challenges then? Why hasn't this happened to any significant level, or has it?***

FLORES: The challenge is that there are a lot of sunk costs in applications already within the government. And so if you want to have an application that natively understands a cloud, then it has to be written for that. And so that requires a whole different level of skill and programming to do that. Things like Appistry come along and, as mentioned, they preclude you from having to do that.

And the defense industry is very excited about cloud computing. For a long time, the scientific community had what they called "grid computing." And so that was a similar kind of concept but not really the same thing. With grid computing, you were actually reliant on the hardware that you had in place, and up until recently you didn't really have this virtualization concept that came into play. But that's the whole beauty of "the cloud."

MIL EMBEDDED: ***How fast do you think the DoD will really adopt cloud computing in a forward-moving way?***

FLORES: The key thing in all of this is that the big brass in the DoD world for the most part gets it. And so they're pushing from the top to make this happen, and then the geeks in the basement are pushing from the bottom to make it happen. And that's the fastest way to get anything done within the government, believe me.

MIL EMBEDDED: ***It'd be interesting to find out how this might affect the primes and subs in the middle. Can they actually go out to a COTS company like Appistry and say, "Well gee, it actually exists and we don't have to write this from scratch. There go our IDIQ contracts…"***

FLORES: That, frankly, is an issue with some of the integrators, and that's where it takes some very strong leadership from the contracting officers within the government.

MIL EMBEDDED: ***What's the biggest challenge then for Appistry in this market space? Is it getting the word out? Is it convincing the system integrators?***

FLORES: In my view, it's not a technology challenge, it's more of a fiscal challenge.

It requires "new think," and new think requires new contracts. And there have been a lot of cuts. So the agencies, particularly the intel and DoD agencies, unless they particularly apply to the efforts in theater, they're under a lot of scrutiny and pressure to keep costs down. The government works in one- and two-year money blocks. For them, the ROI has to happen (in the case of the intelligence agencies) within a year, in the case of DoD within two years.

We have to remember that for the most part, the existing working budgets were defined three years ago and sometimes can't change rapidly to reflect new ideas.

Bob Flores *is the Founder and President of Applicology Incorporated, an independent consulting firm specializing in informatics and cyber security issues. Prior to starting Applicology, Bob spent 31 years at the Central Intelligence Agency where he held various positions in the Directorate of Intelligence, Directorate of Support, and the National Clandestine Service. Toward the end of his career at the CIA, he spent three years as the CIO's Chief Technology Officer, responsible for ensuring that the Agency's technology investments matched the needs of its mission. During this time Bob was also the Agency's representative on several government-wide information-sharing committees and councils. In addition to his senior-level leadership and management positions, his career included assignments in applications programming, training and education, contract and project management, and line and staff management roles at various levels of the Agency. He holds Bachelor and Master of Science degrees in Statistics from Virginia Tech. He can be contacted at bob.flores@applicology.com*

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Bob Lozano *is an experienced entrepreneur, author, and cofounder of Appistry, a provider of cloud application platforms. Bob serves as Chief Strategist, after being the founding CEO. Bob previously founded and led PaylinX, a pioneer and leader in ecommerce payments (acquired by CyberSource {CYBS} in 2000). Prior to PaylinX, Bob founded several additional companies and held positions with SBC (AT&T), Monsanto, Sandia National Laboratories, and Intelligent Computer Systems. Bob holds a BSEE from the University of Missouri and an MSEE from Stanford, and has lectured on artificial intelligence at Washington University in St. Louis. He is the co-author of "Executive's Guide to Cloud Computing" (Wiley, April 2010). He can be followed on twitter at boblozano or contacted via email at bob@appistry.com.*

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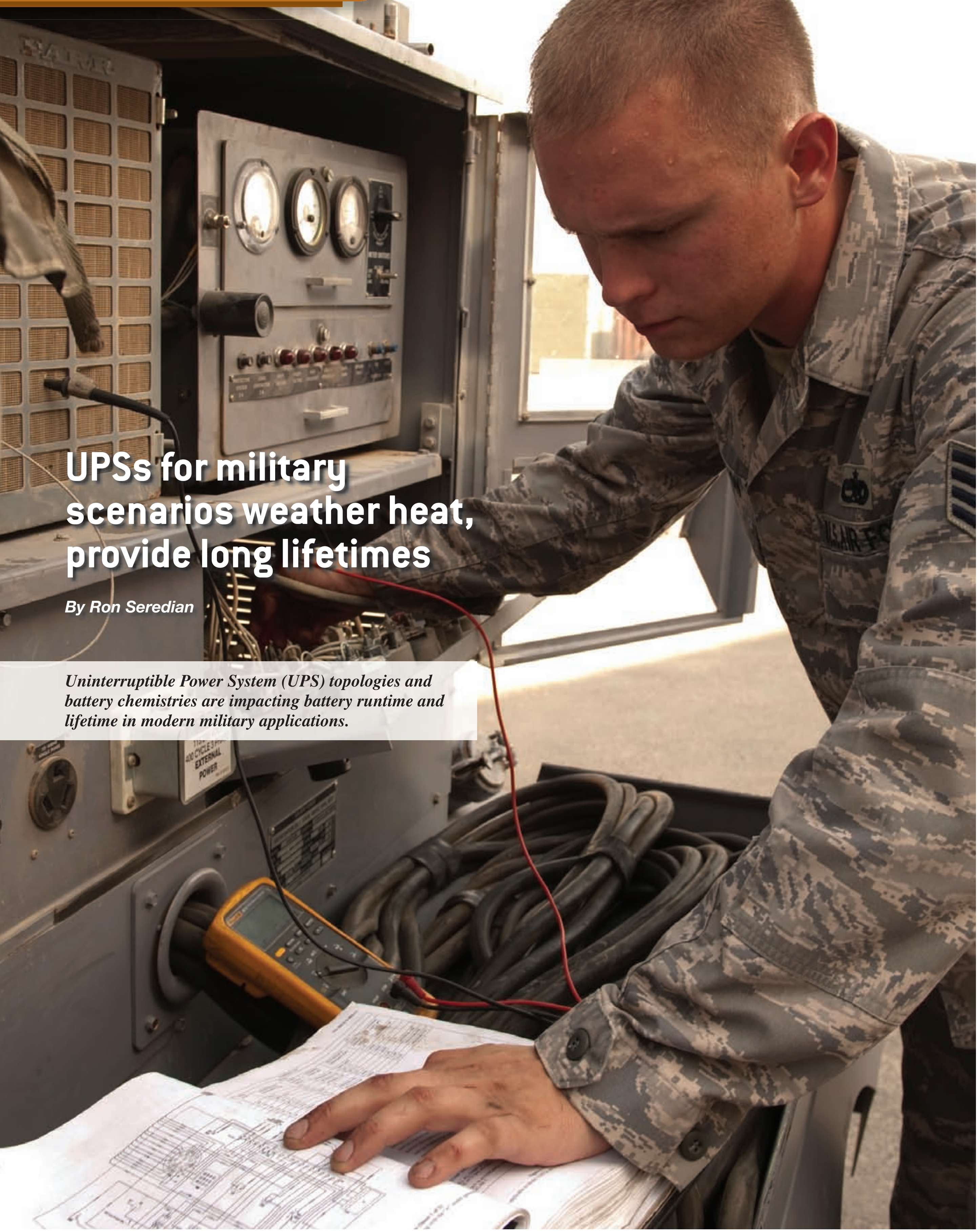


U.S. Air Force photo by Staff Sgt. Robert Barney

UPSs for military scenarios weather heat, provide long lifetimes

By Ron Seredian

Uninterruptible Power System (UPS) topologies and battery chemistries are impacting battery runtime and lifetime in modern military applications.

There's still truth to the classic remark attributed to Napoleon Bonaparte: "An army marches on its stomach." Today's military runs on electric power (and also still on its stomach). But while food can be brought in from outside sources, AC power must be obtained either from local utilities or from closeby generators. And compared to power supplied by utilities throughout most of the United States and many other countries, the local or generator power provided in many military locations is subject to many problems. Among these issues are 1) brief or prolonged "brownouts" – sags in voltage levels, which can also be caused by excessive demand by other devices; or 2) outages – periods of seconds or minutes with no power at all.

If not prevented or mitigated, these AC power sags and outages can interfere with application or device operations. Other possible ramifications include scrambled data and damaged hardware, which in turn increase the potential for mission failure, personnel injury, or even death. To the rescue: Uninterruptible Power Systems (UPSs), which can be used to mitigate these power sags and outages[1]. Meanwhile, a thorough understanding of UPS topology choices and battery chemistries is imperative for proper selection of power alternatives that can offer the longest lifetime possible in today's heat-intensive military environments.

UPSs versus "the old way"

UPS performance requires that the battery retain its ability to hold a charge (capacity), deliver this power as needed, and recharge. One key indicator of battery life and health is the number of discharge cycles the battery is rated for. A typical number is 260 cycles; thus, if batteries are being used in "standby service" – meaning the batteries are rarely cycled or discharged – they should last the full rated life.

Several factors can degrade battery performance and lifetime, particularly: how frequently and deeply a battery is discharged or "cycled," and also temperature. (These circumstances are also likely in many industrial and field-service scenarios.)

Given that these UPSs are often in remote field locations, re-provisioning is often expensive and inconvenient – and might be difficult on short notice. Reprovisioning is also an added expense – on top of the cost of more-frequent fresh batteries and returning, recycling, or disposing of the old ones. Of even greater concern is that an overstressed UPS battery that has not been replaced in time might fail at a critical time, with potentially serious consequences.

However, the good news is that various methods exist to help mitigate excessive battery drain and environmental heat, including:

- Selecting an appropriate UPS topology
- Selecting a more heat-tolerant battery chemistry

[1] Generators or other on-site technologies are needed to address longer utility outages or locations with no utility power available. And UPSs are still advised in concert with a generator.

UPS topology impacts battery lifetime

UPSs come in three topologies: Off-Line, Line-Interactive, and On-Line, each of which has its own unique effect on battery lifetime.

Off-Line UPS

The Off-Line UPS, during utility mode operation using the externally provided power, essentially feeds the utility power directly to its output. Since undervoltage can be as bad for operations as zero power, an Off-Line UPS is designed to transfer to battery mode not only when utility power fails, but also when it drops below a specified level (typically, for a 120 VAC line, 102-105 VAC). This type of drop might occur during a brownout or a sag, for example.

In a location with a sustained low-utility-voltage condition, an Off-Line UPS can continuously transfer into and out of battery mode, resulting in battery overcycling and significantly shortening battery life. Additionally, in some cases the batteries might never have a chance to recharge, rendering the UPS useless.

Line-Interactive UPS

The Line-Interactive UPS incorporates an internal tap-switching transformer circuit, often referred to as an Automatic Voltage Regulation (AVR) circuit. This circuit monitors the utility voltage and, when appropriate, automatically switches transformer taps to increase or lower the UPS output voltage in gross steps, to sustain the target voltage while avoiding going to battery power as much as possible. Depending on the brand and model, the output voltage is maintained between ±12 percent (105.6-134.4 VAC) down to ±5 percent (114-126 VAC) without having to switch to the battery.

While this is an improvement over the off-line design, some line-interactive designs must transfer to battery mode during the tap transfers; thus, in locations with an unstable utility voltage, the batteries are again subjected to overcycling.

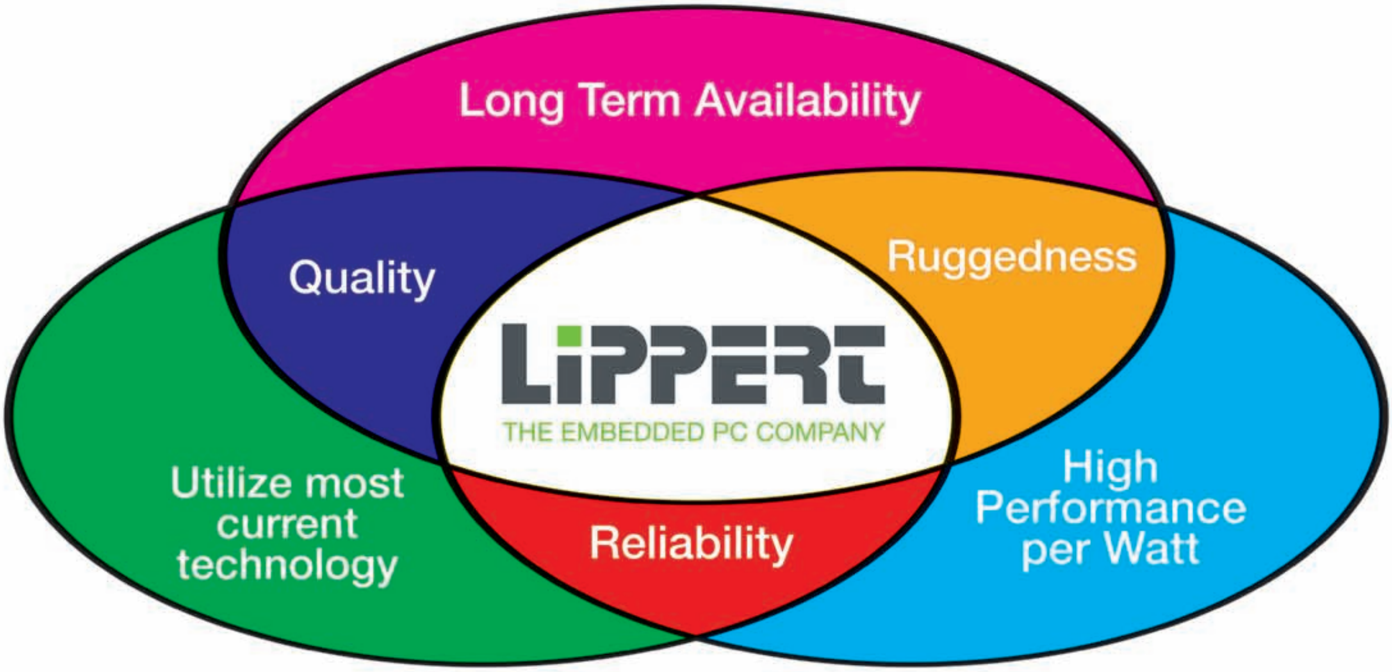
On-Line UPS

The On-Line UPS is also known as "dual conversion" UPS. On-Line UPS converts the utility power to a filtered DC current, which is then electronically regulated and supplies a continuous duty, sine-wave inverter circuit. This inverter, in turn, regenerates new, tightly regulated AC power to its output – typically ±2 percent voltage regulation – hence the "dual conversion."

The On-Line UPS can avoid drawing on the battery, yielding an ever-wider utility voltage range than the Line-Interactive UPS: typically -25 percent to +15 percent or 90-138 VAC. Thus, using an On-Line UPS greatly reduces the number of battery cycles versus the other UPS topologies in locations where the utility power level fluctuates frequently.

Disparate battery chemistries tolerate discharge, heat differently

Heat, whether due to buildup in a small or enclosed space or because of ambient weather, also significantly impacts battery



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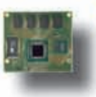

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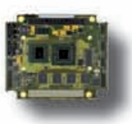

Model	Format	CPU, Clock	RAM (max)	Miscellaneous
CoreExpress-ECO	CoreExpress®	Atom™ 5xx 1.1 ... 1.6 GHz	2 GB soldered	2 x PCI Express, SDVO, USB
Cool XpressRunner-GS45	PCI/104-Express	Core™ 2 Duo	1 GB	LAN, SATA, USB
Cool RoadRunner-945GSE	PC/104-Plus	Atom™ N270 1.6 GHz	2 GB soldered	LAN, 2 GB SSD, SATA
Cool RoadRunner-PM	PC/104-Plus	Pentium® M 0.6 ... 1.8 GHz	1 GB	LAN, USB
Cool RoadRunner-4	PCI-104	Pentium® M 0.6 ... 1.8 GHz	1 GB	LAN, USB
Hurricane-PM	EPIC	Pentium® M 0.6 ... 1.8 GHz	1 GB	LAN, USB, uDoC
Thunderbird	Mini-ITX	Pentium® M 0.6 ... 1.8 GHz	1 GB	LAN, MiniPCI
Thunderbird/MM	Mini-ITX	Pentium® M 0.6 ... 1.8 GHz	1 GB	LAN, USB, uDoC, Mini PCI, DVI, SPDIF, IEEEE1394
Thunderbird-GM45	Mini-ITX	Core™ 2 Duo 2.53 GHz	4 GB	LAN, SATA, USB, Intel® AMT, Adaptive-IO™
Thunderbird-E3100	Mini-ITX	Core™ 2 Duo 1.89 GHz	8 GB ECC	LAN, ASF, SATA, USB, MiniCard

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performance. Insulated enclosures and other design approaches can shield UPS batteries from some heat buildup. Another approach is to use a battery with better heat tolerance.

For well over two decades Valve Regulated Sealed Lead-Acid (VRLA) batteries (which are related to, but not the same as, those found in automobiles, RVs, and boats) have typically been used to provide the backup power for most UPS products. These batteries have the high energy storage capacity needed for UPS applications and are available at a low cost.

The typical usable lifetime of a VRLA battery under normal operating conditions – such as being operated in a 25 °C (77 °F) temperature environment – is three to five years; thereafter, VRLA battery capacity and/or ability to hold a charge might decline below accepted thresholds.

Unfortunately, typical VRLA batteries do not tolerate high temperatures. As the battery gets warmer, its lifetime and storage capacity degrade, as does the maximum current it can output. So instead of getting 15 minutes of backup time during a power outage, the user might only get a few minutes. Also, in a sustained 50 °C (122 °F) environment, the same battery will have a service life of less than one year (see Figure 1).

Within the past few years, improved VRLA batteries with longer life are becoming available from companies including CSB Battery Co., Ltd. (www.csb-battery.com). These new VRLA batteries have up to a remarkable 10-12 year rating at room temperature, and somewhat better heat tolerance levels have become available – with pricing competitive to the traditional five-year VRLA batteries. Additionally, these new VRLA batteries have somewhat better operational life at higher temperatures – up to four years at 50° C. This makes these new VRLA products better matches for UPSs in heat- and power-challenging environments.

In 2009, Falcon Electric introduced the first UPS with long-life, high-temperature batteries. The SSG Series UPS is rated to 55 °C, and the internal batteries are rated to operate for four years at 50 °C. These new batteries, housed inside an enclosure that is inserted into the UPS, are shielded from ambient heat and reduce TCO by significantly extending the traditional battery replacement cycle.

However, like traditional VRLA batteries, these new VRLA batteries' life will be shortened if operated above 25 °C (77 °F), or if the proper charge level is not maintained[2] (Figure 2).

UPSs solve modern military power issues

When looking to purchase a COTS UPS for a specific application, a high-temperature On-Line UPS design is a good place to start. Through its robust design, it represents the best reliability model even if used in a normal ambient temperature application. And the On-Line topology maximizes battery performance in the face of highly unreliable utility power levels and availability. There's no downside to this choice: Particularly where the success of military missions and safety of personnel are at stake, it's the right choice.

[2] The short battery life at elevated temperatures can be mitigated to some degree by implementing good thermal insulation practices during battery-pack design.

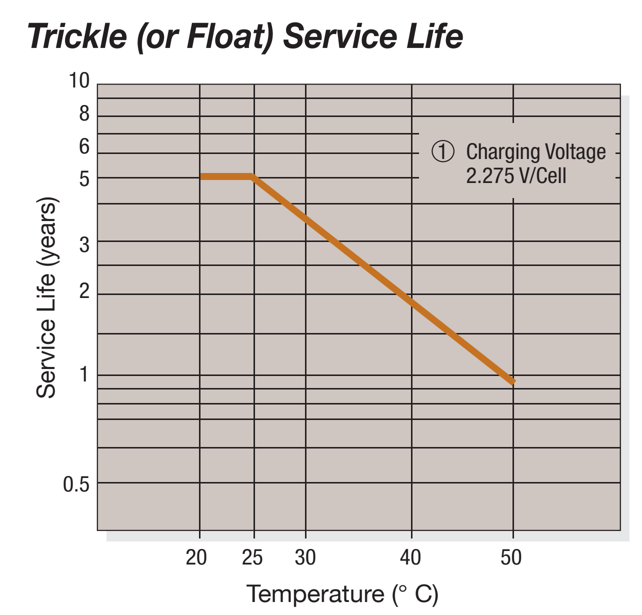


Figure 1 | Typical measurements for 3- to 5-year-rated VRLA batteries

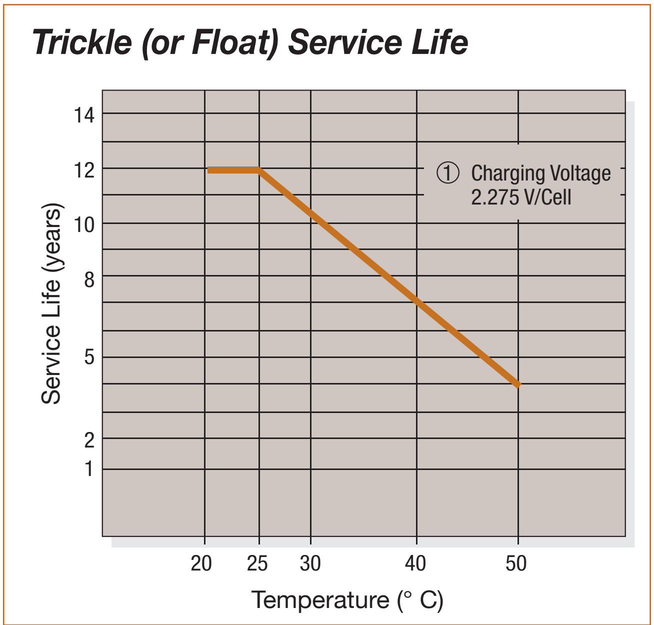
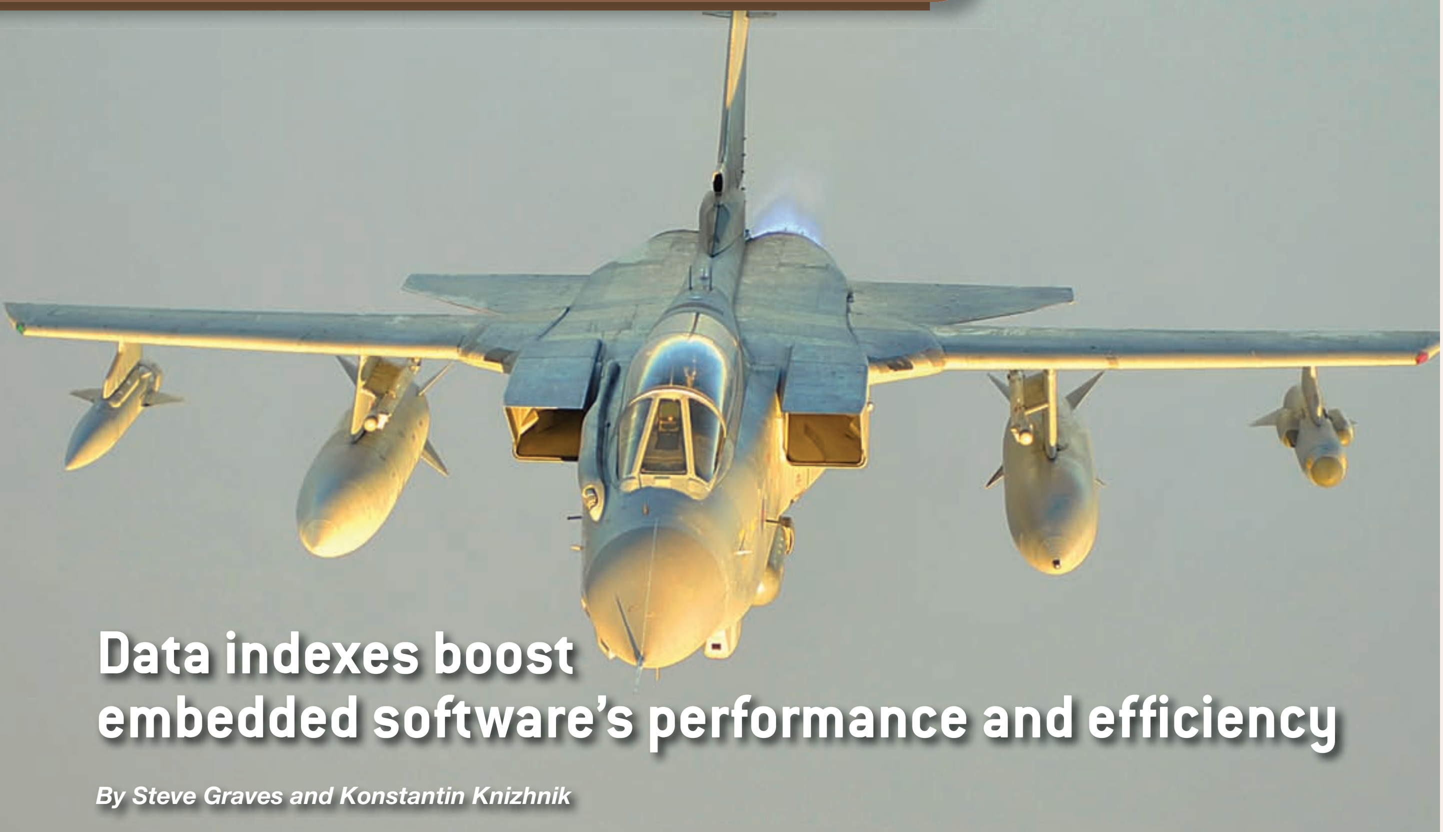


Figure 2 | Typical measurements for 10- to 12-year-rated VRLA batteries

Ron Seredian, *Falcon Electric Inc.'s Vice President of Marketing, has more than two decades of experience in the power conversion industry, both in the U.S. and in Europe. He has written many articles on the topic of power protection and holds a Bachelor of Science degree in Marketing from California State University, Northridge.*

Falcon Electric, Inc.
800-842-6940 • www.falconups.com



Data indexes boost embedded software's performance and efficiency

By Steve Graves and Konstantin Knizhnik

U.S. Air Force photo by Staff Sgt. Aaron Allmon II

Use of a data index can improve an embedded application's lookup speed an order of magnitude over linear search. The best-known general-purpose index is the B-Tree, but specialized indexes such as R-Trees and Patricia tries are ideal for many diverse application functions such as mapping and IP filtering.

To find information in a book, what makes more sense: reviewing every page for the sought-after content, or consulting the index, to discover exactly where to look?

Surely the latter makes more sense, and embedded software should be equally smart. Today's embedded applications manage increasing volumes of complex data. Finding the right data – whether to route network packets, calculate distance to a point on a map, or achieve some other processing goal – typically must be achieved under real-time deadline pressure.

Fortunately, programmers can use data indexes to improve data lookup performance logarithmically over linear search. Use of indexes has increased as off-the-shelf Database Management Systems (DBMSs) have grown to play a larger role in embedded systems development, with most embedded databases supporting one or more index type.

However, in many projects, the first and often the only index considered is the B-Tree. This is because among the large existing variety of indexes, only B-Tree indexes are offered universally. There is no denying B-Trees' efficiency for basic search operations like exact match, prefix, and range searches. However, for purposes as varied as IP routing, mapping, and query-by-form algorithm development, less common index types can be a better fit, resulting in faster performance and more efficient use of processing resources such as CPU cycles (see Sidebar 1).

The following scenarios illustrate how two of the less common index types – the R-Tree and the Patricia trie – are used.

Spatial indexing and the R-Tree

Mapping and other location-based functions are common in mobile and embedded applications ranging from battle support systems in combat vehicles, to mobile phone apps for finding the nearest pizza joint. Such applications are based on algorithms that perform spatial searches such as locating the nearest object to a current location, finding all objects near the user, and so on.

B-Tree indexes are single-dimensional: They can't handle the R2 or R3 coordinates

Indexing choices abound

Other index types worth exploring include KD-Trees (for multi-dimensional data and query-by-example, or QBE, functions), T-Trees for in-memory data access and storage, Hash indexes for quickly locating a single unique index entry, and user-defined or "custom" indexes, which extend a B-Tree to accept the user's specified comparison function. By accessing information that is freely available on the Internet and elsewhere, developers can learn about these index types and can determine, in advance, whether a specific index type is needed for a new application. Support or non-support for that index should be among the criteria used to select a database for the application.

Sidebar 1 | B-Trees are not the only index choice for embedded applications.

used in spatial searches. A much better alternative is the R-Tree, also named *Guttman's R-Tree* after its inventor. It maps objects in space using a "bounding box." If an object is represented by point coordinates (X, Y), then its bounding box is a degenerated rectangle in which the width and height are one.

For all other geographical objects (lines, polygons, and other shapes), the bounding box is such that the top-left corner coordinates are smaller than or equal to the coordinates of any point of the object, and the coordinates of the bottom-right corner are greater than or equal to the coordinates of any point of the object. In other words, a wrapping rectangle is the smallest rectangle that can fully contain a given object.

R-Tree indexes are commonly used to speed spatial searches (to discover the rectangle that bounds a given point, find all rectangles that overlap a given rectangle, and so forth). The application can manage all manner of shapes with help from the bounding box.

Using *eXtreme*DB's database definition language, a spatial object can be described as follows:

```
/* structure representing point on the map */
struct Point
{
    double latitude;
    double longitude;
};

class Street {
    /* vector of points specifying the street */
    vector<Point> points;
    /* Street wrapping rectangle */
    rect<double>  wrap_rect;

    rtree<wrap_rect> streets_idx;
};
```

If we want to add a new street, the application must store the street's coordinates and calculate its bounding box:

```
Street street;
mco_rect_t wr;
wr.l.x = DOUBLE_MAX;
wr.l.y = DOUBLE_MAX;
wr.r.x = DOUBLE_MIN;
wr.r.y = DOUBLE_MIN;
Street_new(trans, &street);
Street_points_alloc(&street, n_points);
for (i = 0; i < n_points; i++)
{
    if (points[i].latitude < wr.l.latitude) {
        wr.l.latitude = points[i].latitude;
    }
    if (points[i].longitude < wr.l.longitude) {
        wr.l.longitude = points[i].longitude;
    }
    if (points[i].latitude > wr.r.latitude) {
        wr.r.latitude = points[i].latitude;
    }
    if (points[i].longitude > wr.r.longitude) {
        wr.r.longitude = points[i].longitude;
    }
    Street_points_put(&street, i, &points[i]);
}
Street_wrap_rect_put(&street, &wr);
```

If a user searches for a location, the mapping application presents the result (streets) in a window that corresponds to a map rectangle with coordinates |<min_longitude, min_latitude, max_longitude, max_latitude>|.

```
mco_rect_t r;
mco_cursor_t c;
MCO_RET rc;
r.l.x = min_longitude;
r.l.y = min_latitude;
r.r.x = max_longitude;
r.r.y = max_latitude;
if (Street_streets_idx_search(trans, MCO_EQ, &c, (double*)&r) ==
MCO_S_OK)
{
    for (; rc == MCO_S_OK; rc = mco_cursor_next(trans, &c))
    {
        Street street;
        Street_from_cursor(trans, &c, &street);
        // display it
    }
}
```

Patricia trie

The B-Tree can locate keys with a specified prefix, for example, finding businesses with names that start "AAA." But some applications must search for keys that represent the longest prefixes of a specified value. The B-Tree can accomplish this, but only by performing several iterations and searching for different prefixes of the specified value, starting from the longest.

A much more efficient index for prefix searches is the Practical Algorithm to Retrieve Information Coded in Alphanumeric trie (from retrieval) also known as *Patricia trie*. A Patricia trie is a variation of a binary tree and typically is used for phone routing and IP filtering. In the first case, given an incoming call and a table of operators with known prefixes, an application must select the right operator to receive the call. In the second case, given IP masks for valid/rejected domains, a received HTTP request should be classified as accepted, rejected, redirected, and so on. The following database schema defines a routing table, with a mask represented by a vector of bits (Booleans).

```
class Route
{
    Vector<bool> dest;
    uint4 gateway;
    uint4 interf;
    uint2 metric;

    unique patricia<dest> by_dest;
};
```

To locate the proper route for the received IP address, the application searches *eXtreme*DB as follows, using a Patricia trie:

```
mco_cursor_t csr;
if (MCO_S_OK == Route_by_dest_index_cursor(trans, &csr)) {
    uint1 mask[4];
    make_mask(mask, ip, 32);
    /* find routes which mask match this IP address */
    if (MCO_S_OK == Route_by_dest_prefix_match(trans, &csr, mask, 32);
        Route route;
        Route_from_cursor(trans, &csr, &route);
        ...
    }
}
```

The following code converts the integer number representing the IP address into an array of bits:

```
void make_mask(uint1* mask, uint4 val, int bitnum)
{
    int i;
    val = val >> (32-bitnum);
    memset(mask, 0, 4);
    for (i = 0; i < bitnum; i++, val = val >> 1)
    {
        mask[i >> 3] |= (val&1) << (i&7);
    }
}
```

The more index choices, the better the results

Knowledge of specialized indexes such as the R-Tree and the Patricia trie enables faster development, more efficient code, and the ability to work with more complex data structures. While the well-known B-tree is sufficient for many "plain vanilla" searching tasks, less well-known indexes can do a better job for specific application and data types: The R-Tree is highly efficient in handling mapping and geospatial data. Additionally, the Patricia trie is ideal for phone routing, IP filtering, and other tasks that must be accomplished by locating keys that represent the longest prefixes of a specified value.

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***Konstantin Knizhnik** is a software engineer at McObject, where he is involved in the development of the* eXtreme*DB embedded database system. He is also the author of several popular open-source projects including the Java-native database management systems Perst and Perst Lite, as well as tools that extend the capabilities of programming languages including Java, C++, and C#. Konstantin can be reached at knizhnik@mcobject.com.*

McObject
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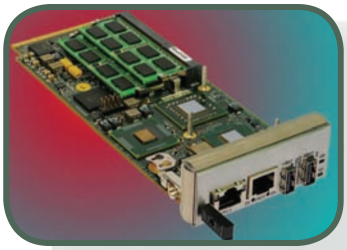
www.mcobject.com

Editor's Choice Products

Editor's note: *Military Embedded Systems is "hip" to the whole Web 2.0 social networking revolution. While we don't know which of today's buzzy trends will last, we're going to start including links to vendors' social networks, when provided. You can also reach us on Twitter, Facebook, and LinkedIn ... and that's just for this week. Next week there'll undoubtedly be more new sites.*



Exploiting the ABCs – and more – of AMCs

The ABCs are taught in grade school as the basic foundation of all learning. In the same vein, Concurrent Technologies recently released its AM 210/x0x AMC processor module, but while the company has employed the "ABCs" of AMCs, they have also taken the concept notably further than just the basics. For starters, this AMC module includes two choices of low-power Intel Core 2 Duo processors: either 1.86 GHz (SL9400) or 2.26 GHz (SP9300). Then there's the plethora of form factors it's suited for: MicroTCA and AdvancedTCA, along with proprietary and Scope Alliance platforms. And its application range is anything but basic: defense, industrial, security, and communications (Voice over IP, wireless base stations, blade servers, and media servers).

Since power is a make-it-or-break-it factor in mil apps and systems, developers will be glad to know that the AM 210/x0x's 2.26 GHz processor version has a Thermal Design Power (TDP) of a mere 25 W … and when melded with the Intel ICH 9M-SFF IO Controller Hub and the Intel GS45 Graphics Memory Controller Hub, what else can result except high performance? And this module can take the heat: Mid- or full-height front-panel versions withstand -25 °C to + 70 °C.

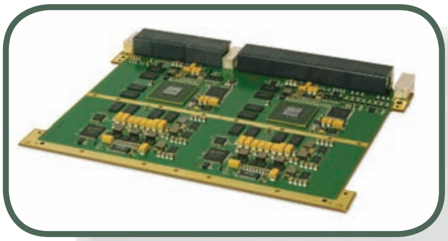
Concurrent Technologies • www.gocct.com • RSC# 44584

OpenVPX/REDI COTS SBC from one of the Big Boys

All single board computers are similar, right? We mean – how many ways can the same components be stuffed onto a board after all? At first glance, the same can be said of the PX3030 by General Dynamics, Canada. Yes, that's right: GD, Canada. That's the difference right there. This 3U VPX/REDI LRU is VITA 46.4, VITA 48.2, and VITA 65 compliant. All that alphabet soup makes this Intel-powered SBC up to snuff with the very latest open standards for rugged VME boards. That's practically unheard of from a prime contractor, which tends to run behind leading edge by months or years. Based upon Intel's 2009 Core 2 Duo ULV in 1.2, 1.86, or 2.26 GHz, the board features system-level features designed for command and control and surveillance applications.

Max memory is a whopping 8 GB of DDR3 SDRAM supported by Intel's GS45/ICH9Me Express chipset. I/O consists of two GbE, two eSATA, six USB, four serial, eight GPIO, RGB, audio, and a VITA 42.3 XMC expansion site. Additionally, the LRU supports 2-level maintenance features as well as an optional IPMI 1.5 subset for local and remote diagnostics and fault indication. There's a TPM onboard for security purposes, a programmable FPGA, and the architecture divides the GbE ports in such a way to facilitate MILS partitioning for mission- and safety-critical systems. You'll find some of these features on many SBCs; finding them *all* on one 0.85-inch pitch SBC (and many more) showcases the board's big-iron vetronics roots in platforms like the M1A2, Palladin, and M777 towed 155 mm artillery piece. By the way – this board is available for sale, even to other primes. It's not just a COTS showpiece done for a lone program.

General Dynamics, Canada
www.gdcanada.com • RSC# 44437



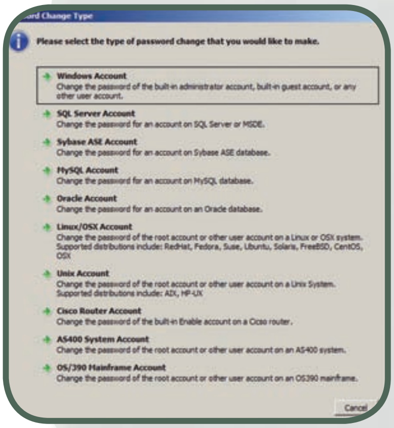
OpenVPX: Bring on the supercomputing

As with most things new (and thus somewhat in the experimental stage), you never know where they will be used … and that's what keeps things interesting. Case in point: We hear about military "supercomputing" from time to time, but this is probably the first time we've heard about it paired with OpenVPX (VITA 65). The embodiment: GE Intelligent Platforms' NPN240 6U OpenVPX CUDA-capable multiprocessor. Armed with two 96-core NVIDIA CUDA-enabled GPUs, the rugged OpenVPX and VPX-REDI (VITA 48) platform can execute at up to 750 GFLOPS peak per card slot. And, to boost the supercomputing exponentially: Several NPN240s can link with multiple hosts (or sometimes even a single host), resulting in multi-node CUDA GPU clusters rendering thousands of GFLOPS. This computational density comes in handy in SWaP-constrained apps, including sonar, radar, video and graphics imaging, and sensor/signal processing too.

Compatible with any OpenVPX host SBC, NPN240 also features parallel GPGPU (General Purpose computing on a Graphics Processing Unit) processing, touted by the company as a more cost-effective alternative to utilizing FPGA-based technologies. Other notables include each GPU node's 16-lane PCI Express gen2 system-backplane interface and local DDR3 SDRAM, along with NPN240's harsh-environment-savvy conduction-, spray-, and air-cooling options.

GE Intelligent Platforms • www.ge-ip.com • RSC# 44580

Random Password Manager is no "con," though it's earned one

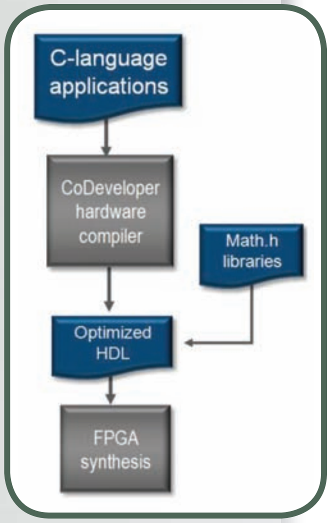


With hackers and even terrorist organizations attempting to breach computer systems and networks on a daily basis, the DoD must protect its data with vice-like tenacity. One way the U.S. Army ensures security for enterprise software wares operating on its Army Enterprise Infrastructure network is by issuing a "CoN" or Certificate of Networthiness (ironically, to eliminate "cons" and security breaches). Accordingly, Lieberman Software Corporation's Random Password Manager privileged identity management product recently received the U.S. Army CoN.

Random Password Manager "automatically randomizes local administrator and root account passwords across every system in the enterprise." It also permits temporary, on-demand recovery of current passwords. Additionally, unique account credentials are maintained by each system so that a decrypted local password cannot render unrestricted entire-network access. These missions are accomplished via a wide variety of features, likely the same ones that caught the U.S. Army's eye: 1) Password recovery – Thanks to a secure Web interface, local passwords can be temporarily checked out by users; 2) Hardware encryption – Hardware-based encryption can be used to reach FIPS 140-2 level 2 and 3 encryption, using any PKCS#11 hardware provider; 3) Firecall accounts – Automated password randomization shields firecall accounts; and 4) Automatic resets, where passwords are re-randomized via a Web interface once the user has checked them in, among myriad other features.

Lieberman Software Corporation • www.liebsoft.com • RSC# 44582

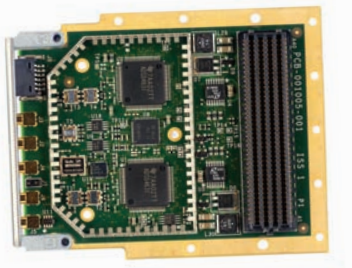
FPGA development library speeds things up



Libraries are known as an excellent venue for information and resources, and software libraries also aim to follow this axiom. A prime example is Impulse Accelerated Technologies Inc.'s Impulse C FPGA math.h Library. The FPGA math.h Library accelerates development of FPGA-based algorithms and also extends the company's Impulse C software-to-hardware compiler's math operations. Many of the library's functions include 32-bit single- or 64-bit double-precision floating-point number use.

One strong advantage of the Impulse C FPGA math.h Library is that it provides function prototypes in the standard C language, thus C programmers will find FPGA math.h easy to use with the same C function calling methods they're already accustomed to. Not only that, the library comprises HDL files and compatible configuration files to make common mathematical operations a breeze … or relatively so, anyway. Meanwhile, other notables of the Impulse C FPGA math.h Library are: risk reduction because of known-good code reuse; retention of ANSI C compatibility when debugging at the software level; and full pipelining for high throughput rates.

Impulse Accelerated Technologies Inc.
www.ImpulseAccelerated.com
RSC# 44382



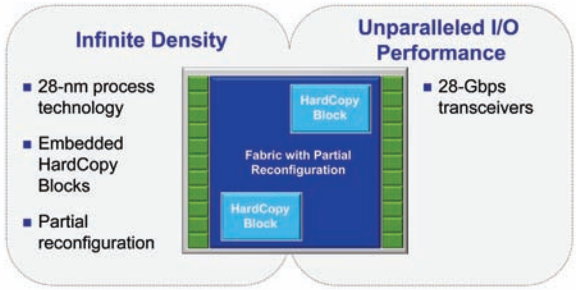
ADC FMC card runs faster, jumps higher

Apparently feeling the need for speed, Curtiss-Wright has actually done the seemingly impossible: achieve the "run faster, jump higher" paradigm. The evidence is its newly tweaked ADC510 FPGA Mezzanine Card (FMC/VITA 57), which does, in fact, run faster (though we're not sure about the "jump higher" part ...). Primary enablers of the ADC510's faster pulse are its two "enhanced" ADS54RF63 Texas Instruments ADCs, which yield a 550 MSps rate with analog bandwidths of >1.7 GHz, rendering 12-bit digital output. Thus, the performance rise between old and new is significant: The former version sampled at 500 MSps and provided analog bandwidths of up to 1.5 GHz.

Meanwhile, other plusses of the ADC510, well suited to SIGINT and SDR apps, include its FMC form factor, for example. Well-known for its I/O simplification, FMC is also only half as big as a PMC, thus meeting modern demand for more SWaP-appropriate wares. Additionally, though the sampling speed now maxes at 550 MSps, those wanting to choose their sample clock sources can opt for onboard clock generator rates of 300, 320, 400, or 500 MSps. Not only that, the number of input channels can be increased when multiple ADC510 modules are synchronized, thanks to the ADC510's output and input triggers.

Curtiss-Wright Controls Embedded Computing • RSC# 44583 • www.cwcembedded.com

FPGAs evolve from 32 ... to 28



As technology grows, chip sizes, of course ... shrink. And FPGAs are no exception to this Moore's Law-motivated phenomenon. Take Altera's new 28-nm FPGAs, for example, to be incarnated with a little help from the company's two recent innovations: Embedded HardCopy Blocks and embedded 28 Gbps transceivers.

First, the Embedded HardCopy Blocks are slated to provide a new partial reconfiguration method. Partial reconfiguration means that designers can reconfigure some FPGA portions at the same time as other sections continue running, increasing system uptime without service disruption. Partial reconfiguration enabled by Embedded HardCopy Blocks will also improve logic density's effectiveness by allowing external memory storage of FPGA functions not presently needed – but which can be uploaded later when required – to free up board space and lower power consumption. Second, Altera's 28 Gbps embedded transceivers, which will ride inside the company's new 28 nm FPGAs, allow 400G system designs on a single chip and thereby eliminate the need for expensive external components. Sounds like a good deal to us.

Altera • www.altera.com • RSC# 44581

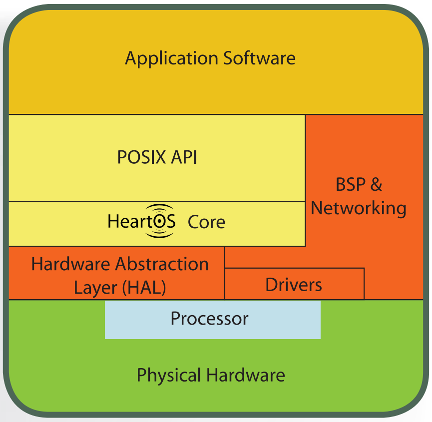
JTAG debug interface for Atom

The Atom processor – with its small size and equally small power consumption – is attracting a lot of attention in modern SWaP-constrained military electronics. And as with any relatively new product, its burgeoning ecosystem needs to match its growing popularity, lest development and market adoption be hindered. However, Macraigor Systems, a provider of debug support in JTAG style, is doing its part to eliminate any Atom processor utilization roadblocks. The evidence: its OCDemon on-chip debug technology, which recently expanded to support the Intel Atom processor.

OCDemon for the Intel Atom is well-suited for providing bootcode and firmware debugging. The JTAG interface connects the host system's debugger to the target hardware, resulting in access to IA-specific capabilities for SoC and chipset peripheral register content, along with execution trace support. These on-chip features can be accessed through several communication channels. And the plan comes together when "a host debugger communicates with a Macraigor Systems' device and then to the target processor." This method can be utilized for application software, kernel, and driver debug, and hardware initialization and debug because the OCDemon eliminates the need for resident code.

Macraigor Systems • www.macraigor.com • RSC# 44451

DDC-I RTOS fills nontrendy ARM niche



When you think of ARM, your first related thought is probably of the Android OS, written for the ARM architecture. And with 10 billion ARM7 and 5 billion ARM9 processors shipped to date, undoubtedly many of the devices have been tucked inside cell phone and consumer mobile gadgets galore since ARM7's 1990s creation. However, DDC-I has a different vision of ARM7 and ARM9's potential: safety- and mission-critical *nonmobile* apps suited for the avionics (especially DO-178B certification-related), industrial automation, transportation, and even medical realms. The enabler is its HeartOS RTOS, compatible with the ARM7 and ARM9 processors.

The deterministic, lightweight HeartOS kernel renders POSIX scheduling, mutexes, threads, message queues, semaphores, threads, condition variables, and clocks and timers. Facilitating these functions and more are HeartOS's POSIX profile 51 interface and profile 52 features including socket communications, among others. Though HeartOS is targeting small- to mid-sized applications, it has a deterministic TCP/IP stack for ... Internet connectivity. That might serve as miniscule proof that DDC-I's HeartOS RTOS hasn't *completely* eschewed the ARM architecture's Internet-everywhere trend.

DDC-I, Inc. • www.ddci.com • RSC# 42771

Crosshairs Editorial

Safety or security? An embedded wake-up call from Toyota's misfortunes

By Chris A. Ciufo, Editor

It started with the Camry that allegedly "surged" with no apparent accelerator input from the driver. Before long, the media reported customer complaints against many Toyota products from Corollas to the vanguard Prius and even some Lexus models. As we went to press, the only things certain about Toyota's drive-by-wire vehicles are that the Feds are poking around, Toyota's lost face (and revenue), and digital electronics in vehicles need to be thought of the same way as avionics systems controlling a Boeing 777 at 35,000 feet. Safety-critical systems – which certainly *ought to include automobiles* – demand special attention by embedded developers.

I've got my own special story to tell about how software in a vehicle can ruin one's day, and damn near killed me. I owned a 2003 Chevy Silverado pickup with all the digital toys. The memory feature on my electric seat frequently went berserk and motored me all the way forward, often unexpectedly smashed against the steering wheel at 60 mph. Turns out a software fix for the *body control module* was needed, except GM engineers were busy doing other things for a full 12 months. In the meantime, I yanked the wire (not the fuse, which would've disconnected the mirrors and other essential electrics). It's estimated that several hundred microcontrollers or microprocessors are found in every modern vehicle. When code goes haywire, does the vehicle end up in a ditch – or worse?

On the other hand, with so much software controlling life's everyday conveniences like cars, cell phones, medical monitors, and the world's banking systems atop the Internet, have we yet come to grips with *embedded* security? Worrying about the latest DDoS attack on a server is commonplace – just ask the political leadership of Estonia how their banking system was shut down by foreign hackers. But you should also be terrified at what a bad actor could do with access to your life via an iPhone – or your automobile.

According to Robert Dewar, Emeritus Professor of Computer Science at New York University and President of AdaCore software, there's a big difference between *safety* and *security*. A secure embedded system needs to have assurance of meeting security constraints per an established profile, while a safety-critical system needs to *always* work. For example, the NSA's Tokeneer Project established the requirements for a secure biometric door entry system, and used COTS software with formal methods to establish *and prove compliance* to the security profile (details, including all the code written in SPARK Ada: www.adacore.com/tokeneer).

In the defense industry, myriad standards exist for developing secure software and systems, including separation kernels in operating systems, Multiple Independent Levels of Security (MILS), and time- and space-partitioned environments per ARINC-653, to name just a few. But are these ever used in commercial applications? Doubtful.

Similarly, for safety-critical systems such as avionics, the FAA's DO-178B (software) and DO-254 (hardware) establish criticality levels and formal proof methods to absolutely guarantee that software and systems behave 100 percent predictably. It also follows that every safety-critical system must be secure, because unauthorized access might compromise safety.

My hope would be that secure or safety-critical applications – including smartphones and automobiles – would consider some of our industry's COTS products. I'm sure Wind River or Green Hills will call me and tell me how VxWorks-178 or INTEGRITY-178 is used in a non-military application, but we rarely hear about these installations. It's also likely that the heavy requirements management, formal methods, and NIAP certifications from our world might be "over-kill" in civilian apps.

Still, there's hope. Open Kernel Labs, a company I first became familiar with last year, sells OS kernels for high-volume, low-cost platforms including cell phones. Their OKL4 kernel has *doubled* in volume from 250 million in 2009 to an estimated 500 million handsets for 2010. But it's not just any old kernel – OKL4 creates "secure cells" into which handset applications can run. If one app dies, or goes rogue, it can't spill over or affect the other cells. This is 100 percent identical to the original Green Hills concept of a "padded cell," which coincidentally is the basis for ARINC-653 and other partitioned military environments. Interestingly, OK Labs is unfamiliar with the DoD concepts we all are so familiar with – but the company is clearly following the same path.

As we went to press, OK Labs was scheduled to announce a secure VoIP application running in a secure "hypercell" on a single-core cell phone processor, virtualizing the applications while keeping them separate. This follows the company's Nirvana phone concept – another partitioned application that extends cloud computing to the handset. I am hopeful that as OKL4's security gains traction, the commercial world will wake up to the risks and take a glance at our market and find some inspiration.

But on the safety-critical side, I'm unaware of any U.S.-based civilian efforts mirroring DO-178B. I suspect if anything's happening, it probably will emerge out of Europe's mass transit industry. (If you know of civilian safety-critical activities, drop me a line at cciufo@opensystemsmedia.com and I'll be sure to print it.)

Safety and security are both hugely complicated subjects and ones we routinely cover in *Military Embedded Systems*. Yet ample standards, resources, and tools exist ranging from MILS to DO-178B, to ARINC-653 and DO-254, all the way to static analysis and code verification suites. Any of these could improve tomorrow's generic, nondefense embedded systems. With Intel's goal of "15 billion mobile Internet devices" by 2015 – including automobiles – how much longer can we ignore the issues of security and safety?